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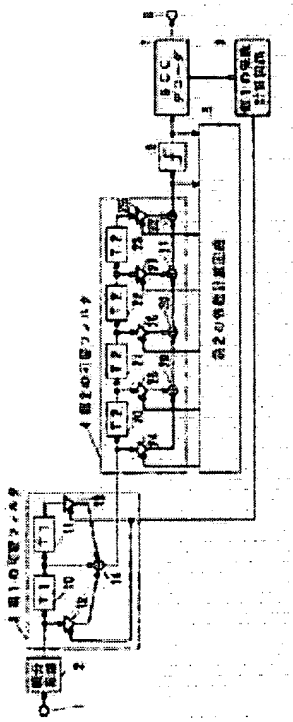
(54) EQUALIZING CIRCUIT

(57)Abstract:
PURPOSE: To execute exact equalization with hardware which is easily reliable and is little.
CONSTITUTION: Variable filters of automatic equalizing circuits are separated to two stages; the first variable filter 3 and the second variable filter 4 to avert the deterioration in frequency by multi-stage series connection of a delay circuit. A difference is afforded to the coefft. convergent time of two stages of the automatic equalization circuits, by which two stages of the automatic equalization circuits are averted from adversely affecting the convergence of the coeffts. on each other. The first variable filter 3 is varied only in its frequency amplitude characteristic by one coefficient A on a phase line. The coefft. A of the variable filter 3 is so updated as to minimize the error flag number from an ECC decoder 7. The total number of taps necessary for obtaining the same equalization characteristics is decreased by changing the delay time between taps of the two transversal filters 3, 4.



MACHINE TRANSLATION OF: JP-H08-161832

CLAIMS

[Claim(s)]

[Claim 1]An equalizing circuit which equalizes a digital signal transmitted or reproduced using a digital filter, comprising:

The 1st variable filter that equalizes an input signal according to the 1st filter factor group into which it is inputted from the outside, and outputs the 1st equalization signal.

The 2nd variable filter that equalizes said 1st equalization signal according to the 2nd filter factor group into which it is inputted from the outside, and outputs the 2nd equalization signal.

An identification device which identifies said 2nd equalization signal and outputs reproduction digital data.

The 2nd coefficient calculating means that updates the 1st filter factor group accommodative, updates the 2nd filter factor group accommodative using the 1st coefficient calculating means and said reproduction digital data outputted to the 1st variable filter, and is outputted to the 2nd variable filter using said reproduction digital data.

[Claim 2]The equalizing circuit according to claim 1 where convergence time of a filter factor in said 1st coefficient calculating means is characterized by a long time rather than convergence time of a filter factor in said 2nd coefficient calculating means.

[Claim 3]The equalizing circuit according to claim 1 characterized by not performing renewal computation of the following coefficient until convergence time of a filter factor in said 2nd coefficient calculating means passes, immediately after said 1st coefficient calculating means updates a filter factor.

[Claim 4]The equalizing circuit according to claim 1 which detects having been completed by each tap coefficient [in / in said 2nd coefficient calculating means / said 2nd variable filter], and outputs a detection result and where said 1st coefficient calculating means is characterized by performing renewal computation of the following coefficient in response to said detection result.

[Claim 5]The equalizing circuit according to claim 4 when variation per unit time of each of said tap coefficient is detected and said 2nd coefficient calculating means becomes [variation of all the tap coefficients] smaller than a predetermined value, wherein it outputs said detection result.

[Claim 6]Detect an error of said reproduction digital data and an error detection decoder which outputs an error flag is provided, The equalizing circuit according to claim 1 to 5, wherein said 1st coefficient calculating means updates said 1st filter factor accommodative and outputs to said 1st variable filter using an error flag outputted from said error detection decoder.

[Claim 7]The equalizing circuit according to claim 1 to 6 where said 1st variable filter is characterized by only a frequency amplitude characteristic being variable in a phase straight line.

[Claim 8]Said 1st variable filter and the 2nd variable filter comprise the 1st transversal filter and 2nd transversal filter, respectively, The equalizing circuit according to claim 1 to 7, wherein a time delay between taps of said 1st transversal filter differs from a time delay between taps of the

2nd transversal filter.
[Claim 9]The equalizing circuit according to claim 8 having set a time delay between taps of said 1st transversal filter as Tb/2 (1 clock period of a digital signal into which Tb was inputted), and setting a time delay between taps of said 2nd transversal filter as Tb.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention enables it to realize exact equalization by small-scale hardware especially about the equalizing circuit which compensates automatically degradation received in the case of transmission and the reproduction from recording equipment of digital information.
[0002]
[Description of the Prior Art]In order to improve the reliability of a regenerative signal conventionally to the signal reproduced with the digital magnetic recorder and reproducing device, Carrying out automatic equalization of the frequency characteristic using an equalizing circuit is performed (for example, Mita, Ide, Inagaki: the simple automatic equalizer for digital video tape recorders, Proceedings of Workshop of the Institute of Television Engineers of Japan, 13 volumes, No. 59, 7-12 pages, VIR'89 1989 [-20 or]).
[0003]The integration circuit 45 which outputs the integral waveform of the regenerative signal to input as this equalizing circuit is shown in drawing 4, The transversal filter 46 which performs equalization processing to an input signal, and the discrimination decision circuit 55 which discriminates digital data from the equalized outputs of the transversal filter 46, and is reproduced, The coefficient calculation circuit 56 which calculates the update values of the coefficient in the transversal filter 46 from the equalized outputs of the transversal filter 46 and the reproduction digital data of the discrimination decision circuit 55 is comprised, The delay circuits 48 and 49 where, as for the transversal filter 46, a digital signal 1-clock-period-Tb[every]-delays an input signal, It has the variable gain amplifiers 50, 51, and 52 which amplify a signal with the amplification factor of the updated coefficient, and the adding machine 53 which adds the output of each variable gain amplifiers 50-52, and is outputted as equalized outputs.
[0004]The reproducing output of the playback head 42 which played the digital signal recorded on the magnetic tape 41 inputs into the input terminal 44 of this equalizing circuit 43.
[0005]As a solid line shows, as for the signal spectrum of the signal outputted from this playback head 42, the low-pass frequency component shows drawing 5 the differentiation characteristic. That is, in a magnetic-recording reversion system, it is not reproduced, but the electric power of a dc component contained in a regenerative signal decreases, so that frequency is low. The electric power of a high region frequency component reproduced decreases by the various losses of gap loss, spacing loss, etc.
[0006]For this reason, in order to return a regenerative signal to a digital code with high reliability, it is necessary to perform exact equalization. This is realized by equalizing so that the frequency characteristic of a regenerative signal may be brought close to what is called roll-off characteristics (the dashed line showed an example to drawing 5).
[0007]A low-pass frequency component is compensated in the integration circuit 45, and the

signal which returned to drawing 4 and was inputted into the input terminal 44 is inputted into the transversal filter 46.

[0008]In the transversal filter 46, the variable gain amplifier 50 amplifies the signal inputted into the input terminal 47 with the amplification factor of coefficient-C_{-1} (however, when a coefficient is a negative value). The variable gain amplifier 51 which shall reverse the polarity of an input signal, The input signal with which only 1 clock-period Tb was delayed in the delay circuit 48 is amplified with the amplification factor of coefficient-C_0, and the variable gain amplifier 52 amplifies the input signal with which only 1 clock-period Tb was delayed to the pan in the delay circuit 49 with the amplification factor of coefficient-C_{+1}. Inputting the output signal of each variable gain amplifiers 50-52 into the adding machine 53, the adding machine 53 outputs equalization signal Y_{-1} which are those aggregate values from the output terminal 54.

[0009]Equalization signal Y_{-1} outputted from the transversal filter 46 is inputted into the discrimination decision circuit 55 and the coefficient calculation circuit 56. The discrimination decision circuit 55 discriminates digital data a_{-1} from equalization signal Y_{-1}, and outputs it to the output terminal 57. This discrimination decision circuit 55 is easily realizable by comparing equalization signal Y_{-1} with predetermined reference level, for example using a comparator.

[0010]Input digital data a_{-1} also into the coefficient calculation circuit 56, and the coefficient calculation circuit 56, As an approximate value of the error of record data and equalization signal Y_{-1}, the error of digital data a_{-1} and equalization signal Y_{-1} is used, The update values of coefficient-C_{-1}, C_0, and C_{+1} are calculated so that this error may converge, and it outputs to each variable gain amplifiers 50-52 of the transversal filter 46.

[0011]The input terminal 61 which equalization signal Y_{-1} inputs as this coefficient calculation circuit 56 is shown in drawing 6, The input terminal 62 which digital data a_{-1} inputs, and the subtractor 63 which outputs error e_{-1} of Y_{-1} and a_{-1}, The delay circuit 64 where only periodic Tb delays this error, and the delay circuits 68 and 69 where only periodic Tb delays digital data a_{-1}, The calculation circuit 65 which calculates the update values of $C_{[}$ which were delayed]-1from error e0 and a-1 , The calculation circuit 67 which calculates the update values of $C_{+1}$from calculation circuit [which calculates the update values of Cof delay circuit 680from error e0 and output a0] 66, and error e0 and output a+1 of delay circuit 69 is comprised.

[0012]Digital data a_{-1} inputted into equalization signal Y_{-1} inputted into the input terminal 61 and the input terminal 62 is given to the subtractor 63, and the subtractor 63 subtracts signal a_{-1} from signal Y_{-1}, and outputs error $e_{-1}=Y_{-1}-a_{-1}$. The delay circuit 64 delays error e_{-1} only the time of periodic Tb. This delayed signal is made into error e_0. The delay circuit 64 gives error e_0 to the calculation circuits 65, 66, and 67, respectively.

[0013]On the other hand, digital data a_{-1} inputted from the input terminal 62 is inputted into the calculation circuit 65 and the delay circuit 68. A pan is made to carry out 1Tb delay, and the delay circuit 68 outputs to it the delay circuit 69 which was made to carry out 1Tb delay of this signal, and was outputted as a_0, and this output inputted as a_{+1}. Therefore, the delaying amounts of digital data a_{-1}, a_0, and a_{+1} are 0Tb, 1Tb, and 2Tb, respectively. These signal a_{-1}, a_0, and a_{+1} are given to the calculation circuits 65, 66, and 67, respectively.

[0014]The calculation circuits 65, 66, and 67 perform the following calculations repeatedly for every time Tb. At a certain time i, signal a_{-1}, a_0, a_{+1}, and error e_0 should input into the calculation circuits 65, 66, and 67, respectively. Coefficient-C_{-1}(i) of the transversal filter [in / at this time / in the calculation circuits 65, 66, and 67 / the time i] 46, Coefficient-C_{-1} (i+1) of the transversal filter 46 in the time (i+1) after only time Tb passes, C_0 (i+1), and C_{+1} (i+1) are calculated by the following three formulas using C_0(i) and C_{+1}(i).

[0015]

$C_{-1}(i+1) = C_{-1}(i)$-alpha-e_0 and a_{-1} (formula 1)
$C_0(i+1) = C_0(i)$ - Alpha-e_0-a_0 (formula 2)
$C_{+1}(i+1) = C_{+1}(i)$ - Alpha-e_0-a_{+1} (formula 3)
However, alpha is a constant which determines the speed of convergence of the value of a coefficient, and is called a convergence factor here. The above-mentioned calculation is repeated for every time Tb, and coefficient-C_{-1} of the transversal filter 46, C_0, and C_{+1} are updated.
[0016]Calculation of such a coefficient of a filter is called the zero horsing method (for example, work besides Miyagawa and edited by Institute of Electronics and Communication Engineers: digital signal processing, Institute of Electronics and Communication Engineers, 233 pages, 1981 (the 9th edition)). Coefficient-C_{-1}, C_0, and C_{+1} are recursively converged on an optimum value by this updating.
[0017]The reliability of a regenerative signal improves by this automatic equalization, and faithful playback of the data recorded on the magnetic tape 41 is attained.
[0018]
[Problem to be solved by the invention]However, complicated hardware is required for the conventional automatic equalization circuit. That is, if it tries to perform exact equalization in this equalizing circuit, the tap numbers of the transversal filter 46 must be increased, but realization of hardware becomes more difficult as tap numbers increase.
[0019]Although it is necessary to transmit digitally and record the video signal of high resolution in recent years, in order to transmit and record the digital signal of such a high data rate, the signal of a broadband must be dealt with also in an equalizing circuit. However, when a signal band spreads, it is difficult to constitute the delay circuit which delays only the same time correctly about all the zones. When the series connection of the delay circuit is carried out to multistage, it is easy to cause delayed degradation of the frequency characteristic of a signal. It was dramatically difficult to constitute conventionally the equalizing circuit which can equalize the digital signal of a high data rate correctly for these Reasons.
[0020]This invention solves such a conventional problem.
Also with the digital signal of the high data rate, it is small-scale and aims at providing the equalizing circuit which can carry out automatic equalization correctly by the easy hardware of realization.

[0021]
[Means for solving problem]So, in this invention, the equalizing circuit which equalizes the digital signal transmitted or reproduced using a digital filter is provided with the following.
The 1st variable filter that equalizes according to the 1st filter factor group into which an input signal is inputted from the outside, and outputs the 1st equalization signal.
The 2nd variable filter that equalizes according to the 2nd filter factor group into which this 1st equalization signal is inputted from the outside, and outputs the 2nd equalization signal.
The identification device which identifies this 2nd equalization signal and outputs reproduction digital data.
The 1st coefficient calculating means that updates the 1st filter factor group accommodative using this reproduction digital data, and is outputted to the 1st variable filter, and the 2nd coefficient calculating means that updates the 2nd filter factor group accommodative using reproduction digital data, and is outputted to the 2nd variable filter.

[0022]The convergence time of the filter factor in the 1st coefficient calculating means

constitutes so that it may become longer than the convergence time of the filter factor in the 2nd coefficient calculating means.
[0023]It constitutes so that renewal computation of the following coefficient may not be performed, until the convergence time of the filter factor in the 2nd coefficient calculating means passes, immediately after the 1st coefficient calculating means updates a filter factor.
[0024]It detects having been completed by each tap coefficient [in / in the 2nd coefficient calculating means / the 2nd variable filter], and a detection result is outputted, and it constitutes so that the 1st coefficient calculating means may perform renewal computation of the following coefficient in response to this detection result.
[0025]The 2nd coefficient calculating means detects the variation per unit time of each tap coefficient, and it constitutes so that a detection result may be outputted, when the variation of all the tap coefficients becomes smaller than a predetermined value.
[0026]The error detection decoder which detects the error of reproduction digital data and outputs an error flag is provided, and the 1st coefficient calculating means updates the 1st filter factor accommodative using the error flag outputted from this error detection decoder, and it constitutes so that it may output to the 1st variable filter.
[0027]The 1st variable filter constitutes so that only a frequency amplitude characteristic may be variable in a phase straight line.
[0028]The 1st variable filter and 2nd variable filter are constituted from the 1st transversal filter and 2nd transversal filter, respectively, The time delay between the taps of the 1st transversal filter is changed with the time delay between the taps of the 2nd transversal filter.
[0029]The time delay between the taps of the 1st transversal filter was set as Tb/2 (1 clock period of the digital signal into which Tb was inputted), and the time delay between the taps of the 2nd transversal filter is set as Tb.
[0030]
[Function]Therefore, since the automatic equalization circuit is divided into two steps, the state where many delay circuits carry out a multistage series connection, and frequency degradation occurs is avoidable. Until it distinguishs between the coefficient convergence time of two steps of each automatic equalization circuit or one automatic equalization circuit converges a filter factor, By suspending calculation of the filter factor of another automatic equalization circuit, the situation which two steps of automatic equalization circuits update a coefficient at the period, and a coefficient converges in the mistaken direction is avoided.
[0031]In one automatic equalization circuit, renewal of the coefficient is performed so that the number of the errors contained in reproduction digital data may decrease.
[0032]The flexibility of the frequency characteristic acquired in an equalizing circuit increases by constituting two steps of automatic equalization circuits from a transversal type variable filter, respectively, and changing the time delay between the taps of this filter in each transversal filter. Therefore, the total tap numbers which are needed in order to acquire the same equalization characteristic are reducible.
[0033]
[Working example]The integration circuit 2 where the equalizing circuit in working example of this invention outputs the integral waveform of an input signal as shown in drawing 1, The 1st variable filter 3 that equalizes an input signal, and the 2nd variable filter 4 that equalizes the output signal of the 1st variable filter 3 further, The discrimination decision circuit 5 which discriminates digital data from the output signal of the 2nd variable filter 4, and is reproduced, ECC decoders 7 which perform the error detection and the error correction of this reproduction

digital data, The 1st coefficient calculation circuit 9 that calculates the update values of the coefficient of the 1st variable filter 3 using the error number which ECC decoders 7 detected, It has the 2nd coefficient calculation circuit 6 that updates the coefficient of the 2nd variable filter 4 using the equalization signal of the 2nd variable filter 4, and the reproduction digital data which the discrimination decision circuit 5 outputted.

[0034]The delay devices 10 and 11 with which the 1st variable filter 3 delays [2 / T_1=Tb/] an input signal (1 clock period of the digital signal into which Tb was inputted), It has the variable gain amplifiers 12 and 13 which amplify a signal with the amplification factor of the coefficient A updated by the 1st coefficient calculation circuit 9, and the adding machine 14 which adds the output signal of each variable gain amplifiers 12 and 13, and the output signal of the delay device 10, and is outputted to the 2nd variable filter 4.

[0035]The delay devices 20, 21, 22, and 23 with which only T_2= Tb delays the signal with which the 2nd variable filter 4 was outputted from the 1st variable filter 3, It has the variable gain amplifiers 24, 25, 26, 27, and 28 which amplify a signal with the amplification factor of the coefficient updated by the 2nd coefficient calculation circuit 6, respectively, and the adding machines 29, 30, 31, and 32 which add the output signal of each variable gain amplifiers 24-28 one by one.

[0036]Next, operation of this equipment is explained.

[0037]First, a low-pass frequency component is compensated in the integration circuit 2, and the signal inputted from the input terminal 1 is inputted into the 1st variable filter 3.

[0038]In the 1st variable filter 3, the variable gain amplifier 12 amplifies the signal inputted from the integration circuit 2 with the amplification factor of a coefficient A (however, when a coefficient is a negative value). Moreover it reverses the polarity of an input signal, the variable gain amplifier 13 amplifies the signal for which only Tb (=T_1x2) was delayed with the delay devices 10 and 11 with the amplification factor of a coefficient A. The output signal of each variable gain amplifiers 12 and 13 is added with the adding machine 14 with the signal with which only T_1 was delayed by the delay device 10, and is outputted to the 2nd variable filter 4.

[0039]With the 2nd variable filter 4, the variable gain amplifier 24 amplifies the signal outputted from the 1st variable filter 3 with the amplification factor of coefficient-C_{-2}, and the variable gain amplifier 25 amplifies the signal for which only Tb was delayed with the delay device 20 with the amplification factor of coefficient-C_{-1}. Similarly, the variable gain amplifier 26 amplifies the output signal of the delay device 21 with the amplification factor of coefficient-C_0, and the variable gain amplifier 27 amplifies the output signal of the delay device 22 with the amplification factor of coefficient-C_{+1}, and the variable gain amplifier 28 amplifies the output signal of the delay device 23 with the amplification factor of coefficient-C_{+2}. Add the adding machine 29 and an output signal with the variable gain amplifiers 24 and 25 the adding machine 30, The adding machine 32 outputs the value adding the output signal of all the variable gain amplifiers 24, 25, 26, 27, and 28 eventually by adding the output signal of the variable gain amplifier 26 to the value further, and continuing it.

[0040]Equalization signal Y_{-1} outputted from the 2nd variable filter 4 is inputted into the discrimination decision circuit 5, and the discrimination decision circuit 5 discriminates digital data a_{-1} from equalization signal Y_{-1}, and outputs it as reproduction digital data. This discrimination decision circuit 5 is the same composition as what was explained by the conventional example.

[0041]Input equalization signal Y_{-1} and digital data a_{-1} into the 2nd coefficient calculation circuit 6, and the 2nd coefficient calculation circuit 6, Using this equalization signal Y_{-1} and digital data

a_{-1}, the value of coefficient-C_{-2}, C_{-1}, C_0, C_{+1}, and C_{+2} is calculated, respectively, and it outputs to the variable gain amplifiers 24, 25, 26, 27, and 28 of the 2nd variable filter 4.

[0042]This composition and operation of the 2nd of the coefficient calculation circuit 6 are the same as what was previously explained by drawing 6, and only the point which the tap numbers of the filter only increased from 3 to 5 is different. Therefore, for every time Tb, the 2nd coefficient calculation circuit 6 follows the zero horsing method, and is the formulas 1, 2, and 3. -- Calculation is repeated and coefficient-C_{-2}, C_{-1}, C_0, C_{+1}, and C_{+2} are updated. As a result, these coefficients are recursively converged on the optimal coefficient value.

[0043]On the other hand, digital data a_{-1} outputted from the discrimination decision circuit 5 is inputted into ECC decoders 7. ECC decoders 7 perform processing of error detection or an error correction to this digital data, and output the digital data which corrected the error from the output terminal 8. At this time, ECC decoders 7 output the error flag which shows the existence of an error, or the thing (it is henceforth described as an error flag) which shows the frequency of error generating equivalent to this to the 1st coefficient calculation circuit 9 in processing of error detection or an error correction. Such ECC decoders are widely used in digital transmission or digital recording now (for example, work besides Eto, the Digital Video record technology, Nikkan Kogyo Shimbun, 13 pages, 1990).

[0044]The 1st coefficient calculation circuit 9 that this error flag inputs, The error frequency counters 91 which count the number of the error flags outputted from ECC decoders 7 as shown in drawing 2 (a), The coefficient generator 96 which outputs a different coefficient for every period to the 1st variable filter 3, The memories 93 and 94 which memorize the count number of the error flag of a different period, respectively, It has the change-over switch 92 which switches the memories 93 and 94 which are mistaken for every period of the and connect with the frequency counters 91, and the judging device 95 which judges a suitable coefficient value based on the value memorized by the memories 93 and 94.

[0045]In order that the coefficient generator 96 of this coefficient calculation circuit 9 may control that operation timing to the error frequency counters 91, the change-over switch 92, the memories 93 and 94, and the judging device 95, As shown in drawing 2 (b), the control signal 81 reversed to predetermined every periodic **T is outputted through the signal wire 98, and the value (82 of drawing 2 (b)) of a coefficient A is changed and outputted to the 1st variable filter 3 according to this cycle. That is, A_1 is outputted to the cycle 84 as a coefficient, and A_2 in which only predetermined value **a is smaller than A_1 is outputted to the cycle 85 as a coefficient.

[0046]The error frequency counters 91 reset a counter value, whenever the control signal to input changes, and they calculate the number of the error flags inputted from ECC decoders 7 during the **T. When this counter value is shown in 83 of drawing 2 (b) and the 1st variable filter 3 performs equalization by coefficient A_1, the error flag of E_1 occurs between time **T, When the 1st variable filter 3 performs equalization by coefficient A_2, it is shown that the error flag of E_2 occurred.

[0047]Number of error flags E_2 which number of error flags E_1 which the error frequency counters 91 counted at the last of the period 84 was stored in the memory 93 via the change-over switch 92, and was counted at the last of the period 85 is stored in the memory 94 via the change-over switch 92. The judging device 95 compares the number of error flags stored in this memory 93 and memory 94, judges coefficient value A_2 corresponding to E_2 with that small value to be a thing near the optimal coefficient value, and outputs a decided result to the coefficient generator 96.

[0048]In the 1st variable filter 3, the same coefficient A outputted to the variable gain amplifiers

12 and 13 from the coefficient generator 96 is given. At this time, the transfer characteristic H (f) of the 1st variable filter 3 is $H(f) = Z^{-1} + A(Z^{0} + Z^{-2})$.
$= Z^{-1}\{1 + 2A\text{-}\cos(2\pi\text{-}T_1/f)\}$ (formula 4)
(However, f:frequency, $Z^{-1} = \exp(-\text{jomega}T_1)$, omega: Angular frequency)
It becomes. Therefore, a phase characteristic serves as a straight line and only a frequency amplitude characteristic changes to change of a coefficient A. At this time, a coefficient A and the error frequency which ECC decoders 7 detect serve as a relation as shown in drawing 2 (C).
[0049]Therefore, when the coefficient generator 96 receives the decided result that the direction of coefficient value A_2 ($<A_1$) has few error flags from the judging device 95, When the coefficient value in which only further predetermined value **a is smaller than coefficient value A_2 is outputted to the next period and the decided result that the direction of coefficient value A_1 has few error flags is received conversely, It is completed as an optimum value by the coefficient A by outputting the coefficient value in which only **a is still larger to the next period, and repeating such operation rather than coefficient value A_1, in it.
[0050]In this way, exact equalization becomes possible when completed as an optimum value by both the coefficient of the 1st variable filter 3 of this equalizing circuit, and the coefficient of the 2nd variable filter 4.
[0051]However, in this circuit, if a coefficient A changes, the frequency spectra of the signal outputted from the 1st variable filter 3 change, therefore the characteristic of the 2nd variable filter 4 will also be combined and will change to it. Therefore, when it mistakes in the stage in the middle of both the coefficient of the 1st variable filter 3 and the coefficient of the 2nd variable filter changing and frequency is detected, a possibility that the relation shown in drawing 2 (C) may stop realizing is between a coefficient A and the error frequency which ECC decoders detect.
[0052]In order to avoid this, when setting time until it is recursively completed as an optimum value by each coefficient of the 2nd variable filter 4 to **Tc as the 1st method, there is the method of setting it as a sufficiently long cycle to such an extent that the influence of **Tc can disregard predetermined periodic **T in drawing 2 (b).
[0053]In the error frequency counters 91, the 2nd methods include the method of making it not calculate an error flag after being reset until time **Tc passes.
[0054]As the 3rd method, it detects having been completed by each coefficient of the 2nd variable filter 4 in the 2nd coefficient calculation circuit 6, A detection result is mistaken, it transmits to the frequency counters 91, and there is the method of constituting so that calculation of an error flag may be started after the error frequency counters 91 check convergence of the 2nd variable filter 4. In this case, in order to detect having been completed by each coefficient of the 2nd variable filter 4 in the 2nd coefficient calculation circuit 6, When the variation between time Tb of each coefficient is detected and the variation of all the coefficients becomes smaller than a predetermined value, a detection result is made to output as that which the coefficient in the 2nd variable filter 4 converged.
[0055]By taking such a means, the convergence time of the 1st variable filter 3 becomes longer than the convergence time of the 2nd variable filter 4, and immediately after changing a coefficient, the 1st variable filter 3 does not perform renewal computation of the following coefficient until the convergence time of the 2nd variable filter 4 passes. As a result, in this equalizing circuit, the 1st variable filter 3 and 2nd variable filter 4 repeat convergence by turns, and it is eventually completed as an optimum value by both the coefficients of both filters.
[0056]Thus, making convergence time of the 1st variable filter 3 longer than the convergence

time of the 2nd variable filter 4, Conversely, if it sees, in the equalizing circuit of working example, it will become possible to use the circuit which operates to the 1st coefficient calculation circuit 9 at a low speed as compared with the 2nd coefficient calculation circuit 6, and the part and realization will become easy.

[0057]Time delay T_1 [in / in this equalizing circuit / the delay devices 10 and 11 of the 1st variable filter 3] (=Tb/2), By changing time delay T_2 (=Tb) in the delay devices 20, 21, 22, and 23 of the 2nd variable filter 4, as shown below, it makes it possible to reduce the total of the required tap numbers in the 1st and 2nd variable filters.

[0058]Drawing 3 shows the frequency characteristic of the 1st variable filter 3. The dotted line in a figure is a case where time delay T_1 of the delay devices 10 and 11 is set as Tb/2.

A solid line is a case where time delay T_1 of the delay devices 10 and 11 is set as T_1=Tb like the delay device of the 2nd variable filter 4.

As a dotted line shows, when time delay T_1 are Tb/2, the peak of a frequency characteristic appears in 1/Tb. On the other hand, when time delay T_1 is Tb, as a solid line shows, the peak of a frequency characteristic appears in 1/(2Tb). The frequency characteristic in the conventional equalizing circuit of drawing 4 which has a delay device of time delay Tb, and the 2nd variable filter 4 of this working example also becomes being the same as that of this solid line, and shows symmetry type by the low frequency wave and high frequency side by making peak frequency 1/(2Tb) into the point of symmetry.

[0059]Therefore, in time delay T_1 of the delay devices 10 and 11 of the 1st variable filter 3 being the same as time delay Tb of the delay devices 20-23 of the 2nd variable filter 4, even if it combines those filters, only the frequency characteristic of the tendency shown in a solid line can be acquired.

[0060]on the other hand, when the time delay in the 1st variable filter 3 is changed with the time delay of the 2nd variable filter 4, various frequency characteristics of the high region zone especially constructed in 1/[from frequency 1/(2Tb)] Tb can be boiled and changed by combining those filters. That is, by changing the time delay of the 1st variable filter 3, and the time delay of the 2nd variable filter 4, the flexibility of an equalization characteristic can be increased, therefore a desired equalization characteristic can be acquired by a small number of taps.

[0061]On the other hand, when the tap numbers of the conventional equalizing circuit of drawing 4 tend to be increased simply and it is going to acquire a comparable equalization characteristic, very many tap numbers are needed. In order that it will be necessary to combine with the increase in tap numbers and to enlarge the scale of the coefficient calculation circuit 56 in this case and and a delay circuit may carry out many series connections, degradation of a frequency characteristic occurs.

[0062]In the equalizing circuit of working example, frequency degradation by the multistage series connection of a delay circuit is avoided by dividing the variable filter of an automatic equalization circuit into two steps of the 1st variable filter 3 and the 2nd variable filter 4.

[0063]When the equalizing circuit of working example provides a difference in the convergence time of the coefficient in two steps of automatic equalization circuits, it avoids that two steps of automatic equalization circuits have an adverse effect on convergence of a coefficient mutually.

[0064]The 1st variable filter 3 of this equalizing circuit has a linear phase characteristic, and it is constituted so that only a frequency amplitude characteristic may change, when a coefficient A is changed. Based on the error flag from ECC decoders, the calculation circuit which updates this coefficient A updates a coefficient so that error generating of a reproduction digital signal may

always serve as the minimum. The calculation circuit of this coefficient can simplify that composition compared with the conventional coefficient calculation circuit.
[0065]By constituting two steps of automatic equalization circuits using a both transversal type variable filter, and changing the time delay between two taps of a transversal filter in this equalizing circuit, respectively, Total tap numbers required in order to acquire the same equalization characteristic are reducible.
[0066]In the equalizing circuit of working example, although the tap numbers of the 2nd variable filter 4 were set to 5, even if it changes these tap numbers, the same effect can be acquired. Although the time delay in the 1st variable filter 3 is set as T_1=Tb/2, this time delay can be made into any value. Although the tap numbers of the 1st variable filter 3 were set to 3 and it was considered as the one number of the coefficients to change, it is not necessarily restricted to this and tap numbers and the number of coefficients to change may be made still larger.
[0067]Although working example described an equalizing circuit which used the zero horsing method, a thing using other algorithms is also the same. This equalizing circuit can use not only reproduction of magnetic recording but optical recording etc. for reproduction of data recorded by other recording principles, or can also be used as an equalizing circuit of digital transmission instead of record.
[0068]
[Effect of the Invention]Since the equalizing circuit of this invention has divided the automatic equalization circuit into two steps, it can avoid frequency degradation by the multistage series connection of a delay circuit, and can realize exact equalization, so that clearly from explanation of the above working example.
[0069]Since one side of two steps of automatic equalization circuits is used as the variable filter into which only a frequency amplitude characteristic is changed in a phase straight line and he is trying to update the coefficient of this variable filter using the error flag from ECC decoders, the composition of the coefficient calculation circuit of this filter can be simplified. Since convergence time of one automatic equalization circuit is lengthened and also [required] it is sufficient for working speed also at a low speed, realization of a circuit is easy for this coefficient calculation circuit.
[0070]By constituting two steps of automatic equalization circuits using a both transversal type variable filter, and changing the time delay between two taps of a transversal filter, Total tap numbers required in order to acquire the same equalization characteristic can be reduced, and circuit structure can be kept small.

TECHNICAL FIELD

[Industrial Application]This invention enables it to realize exact equalization by small-scale hardware especially about the equalizing circuit which compensates automatically degradation received in the case of transmission and the reproduction from recording equipment of digital information.

PRIOR ART

[Description of the Prior Art]In order to improve the reliability of a regenerative signal conventionally to the signal reproduced with the digital magnetic recorder and reproducing device, Carrying out automatic equalization of the frequency characteristic using an equalizing circuit is performed (for example, Mita, Ide, Inagaki: the simple automatic equalizer for digital video tape recorders, Proceedings of Workshop of the Institute of Television Engineers of Japan, 13 volumes, No. 59, 7-12 pages, VIR'89 1989 [-20 or]).

[0003]The integration circuit 45 which outputs the integral waveform of the regenerative signal to input as this equalizing circuit is shown in drawing 4, The transversal filter 46 which performs equalization processing to an input signal, and the discrimination decision circuit 55 which discriminates digital data from the equalized outputs of the transversal filter 46, and is reproduced, The coefficient calculation circuit 56 which calculates the update values of the coefficient in the transversal filter 46 from the equalized outputs of the transversal filter 46 and the reproduction digital data of the discrimination decision circuit 55 is comprised, The delay circuits 48 and 49 where, as for the transversal filter 46, a digital signal 1-clock-period-Tb[every]-delays an input signal, It has the variable gain amplifiers 50, 51, and 52 which amplify a signal with the amplification factor of the updated coefficient, and the adding machine 53 which adds the output of each variable gain amplifiers 50-52, and is outputted as equalized outputs.

[0004]The reproducing output of the playback head 42 which played the digital signal recorded on the magnetic tape 41 inputs into the input terminal 44 of this equalizing circuit 43.

[0005]As a solid line shows, as for the signal spectrum of the signal outputted from this playback head 42, the low-pass frequency component shows drawing 5 the differentiation characteristic. That is, in a magnetic-recording reversion system, it is not reproduced, but the electric power of a dc component contained in a regenerative signal decreases, so that frequency is low. The electric power of a high region frequency component reproduced decreases by the various losses of gap loss, spacing loss, etc.

[0006]For this reason, in order to return a regenerative signal to a digital code with high reliability, it is necessary to perform exact equalization. This is realized by equalizing so that the frequency characteristic of a regenerative signal may be brought close to what is called roll-off characteristics (the dashed line showed an example to drawing 5).

[0007]A low-pass frequency component is compensated in the integration circuit 45, and the signal which returned to drawing 4 and was inputted into the input terminal 44 is inputted into the transversal filter 46.

[0008]In the transversal filter 46, the variable gain amplifier 50 amplifies the signal inputted into the input terminal 47 with the amplification factor of coefficient-C_{-1} (however, when a coefficient is a negative value). The variable gain amplifier 51 which shall reverse the polarity of an input signal, The input signal with which only 1 clock-period Tb was delayed in the delay circuit 48 is amplified with the amplification factor of coefficient-C_0, and the variable gain amplifier 52 amplifies the input signal with which only 1 clock-period Tb was delayed to the pan in the delay circuit 49 with the amplification factor of coefficient-C_{+1}. Inputting the output signal of each variable gain amplifiers 50-52 into the adding machine 53, the adding machine 53

outputs equalization signal Y_{-1} which are those aggregate values from the output terminal 54.
[0009]Equalization signal Y_{-1} outputted from the transversal filter 46 is inputted into the discrimination decision circuit 55 and the coefficient calculation circuit 56. The discrimination decision circuit 55 discriminates digital data a_{-1} from equalization signal Y_{-1}, and outputs it to the output terminal 57. This discrimination decision circuit 55 is easily realizable by comparing equalization signal Y_{-1} with predetermined reference level, for example using a comparator.
[0010]Input digital data a_{-1} also into the coefficient calculation circuit 56, and the coefficient calculation circuit 56, As an approximate value of the error of record data and equalization signal Y_{-1}, the error of digital data a_{-1} and equalization signal Y_{-1} is used, The update values of coefficient-C_{-1}, C_0, and C_{+1} are calculated so that this error may converge, and it outputs to each variable gain amplifiers 50-52 of the transversal filter 46.
[0011]The input terminal 61 which equalization signal Y_{-1} inputs as this coefficient calculation circuit 56 is shown in drawing 6, The input terminal 62 which digital data a_{-1} inputs, and the subtractor 63 which outputs error e_{-1} of Y_{-1} and a_{-1}, The delay circuit 64 where only periodic Tb delays this error, and the delay circuits 68 and 69 where only periodic Tb delays digital data a_{-1}, The calculation circuit 65 which calculates the update values of $C_{[}$ which were delayed]-1from error e0 and a-1 , The calculation circuit 67 which calculates the update values of $C_{+1}$from calculation circuit [which calculates the update values of Cof delay circuit 680from error e0 and output a0] 66, and error e0 and output a+1 of delay circuit 69 is comprised.
[0012]Digital data a_{-1} inputted into equalization signal Y_{-1} inputted into the input terminal 61 and the input terminal 62 is given to the subtractor 63, and the subtractor 63 subtracts signal a_{-1} from signal Y_{-1}, and outputs error $e_{-1}=Y_{-1}-a_{-1}$. The delay circuit 64 delays error e_{-1} only the time of periodic Tb. This delayed signal is made into error e_0. The delay circuit 64 gives error e_0 to the calculation circuits 65, 66, and 67, respectively.
[0013]On the other hand, digital data a_{-1} inputted from the input terminal 62 is inputted into the calculation circuit 65 and the delay circuit 68. A pan is made to carry out 1Tb delay, and the delay circuit 68 outputs to it the delay circuit 69 which was made to carry out 1Tb delay of this signal, and was outputted as a_0, and this output inputted as a_{+1}. Therefore, the delaying amounts of digital data a_{-1}, a_0, and a_{+1} are 0Tb, 1Tb, and 2Tb, respectively. These signal a_{-1}, a_0, and a_{+1} are given to the calculation circuits 65, 66, and 67, respectively.
[0014]The calculation circuits 65, 66, and 67 perform the following calculations repeatedly for every time Tb. At a certain time i, signal a_{-1}, a_0, a_{+1}, and error e_0 should input into the calculation circuits 65, 66, and 67, respectively. Coefficient-C_{-1}(i) of the transversal filter [in / at this time / in the calculation circuits 65, 66, and 67 / the time i] 46, Coefficient-C_{-1} (i+1) of the transversal filter 46 in the time (i+1) after only time Tb passes, C_0 (i+1), and C_{+1} (i+1) are calculated by the following three formulas using C_0(i) and C_{+1}(i).
[0015]
$C_{-1}(i+1) = C_{-1}(i)$-alpha-e_0 and a_{-1} (formula 1)
$C_0(i+1) = C_0(i)$ - Alpha-e_0-a_0 (formula 2)
$C_{+1}(i+1) = C_{+1}(i)$ - Alpha-e_0-a_{+1} (formula 3)
However, alpha is a constant which determines the speed of convergence of the value of a

coefficient, and is called a convergence factor here. The above-mentioned calculation is repeated for every time Tb, and coefficient-C_{-1} of the transversal filter 46, C_0, and C_{+1} are updated.
[0016]Calculation of such a coefficient of a filter is called the zero horsing method (for example, work besides Miyagawa and edited by Institute of Electronics and Communication Engineers: digital signal processing, Institute of Electronics and Communication Engineers, 233 pages, 1981 (the 9th edition)). Coefficient-C_{-1}, C_0, and C_{+1} are recursively converged on an optimum value by this updating.
[0017]The reliability of a regenerative signal improves by this automatic equalization, and faithful playback of the data recorded on the magnetic tape 41 is attained.
[0018]

EFFECT OF THE INVENTION

[Effect of the Invention]Since the equalizing circuit of this invention has divided the automatic equalization circuit into two steps, it can avoid frequency degradation by the multistage series connection of a delay circuit, and can realize exact equalization, so that clearly from explanation of the above working example.
[0069]Since one side of two steps of automatic equalization circuits is used as the variable filter into which only a frequency amplitude characteristic is changed in a phase straight line and he is trying to update the coefficient of this variable filter using the error flag from ECC decoders, the composition of the coefficient calculation circuit of this filter can be simplified. Since convergence time of one automatic equalization circuit is lengthened and also [required] it is sufficient for working speed also at a low speed, realization of a circuit is easy for this coefficient calculation circuit.
[0070]By constituting two steps of automatic equalization circuits using a both transversal type variable filter, and changing the time delay between two taps of a transversal filter, Total tap numbers required in order to acquire the same equalization characteristic can be reduced, and circuit structure can be kept small.

TECHNICAL PROBLEM

[Problem to be solved by the invention]However, complicated hardware is required for the conventional automatic equalization circuit. That is, if it tries to perform exact equalization in this equalizing circuit, the tap numbers of the transversal filter 46 must be increased, but realization of hardware becomes more difficult as tap numbers increase.
[0019]Although it is necessary to transmit digitally and record the video signal of high resolution in recent years, in order to transmit and record the digital signal of such a high data rate, the signal of a broadband must be dealt with also in an equalizing circuit. However, when a signal band spreads, it is difficult to constitute the delay circuit which delays only the same time correctly about all the zones. When the series connection of the delay circuit is carried out to multistage, it is easy to cause delayed degradation of the frequency characteristic of a signal. It was dramatically difficult to constitute conventionally the equalizing circuit which can equalize

the digital signal of a high data rate correctly for these Reasons.
[0020]This invention solves such a conventional problem, it is small-scale also about the digital signal of a high data rate, and an object of this invention is to provide the equalizing circuit which can carry out automatic equalization correctly by the easy hardware of realization.

MEANS

[Means for solving problem]So, in this invention, the equalizing circuit which equalizes the digital signal transmitted or reproduced using a digital filter is provided with the following.
The 1st variable filter that equalizes according to the 1st filter factor group into which an input signal is inputted from the outside, and outputs the 1st equalization signal.
The 2nd variable filter that equalizes according to the 2nd filter factor group into which this 1st equalization signal is inputted from the outside, and outputs the 2nd equalization signal.
The identification device which identifies this 2nd equalization signal and outputs reproduction digital data.
The 1st coefficient calculating means that updates the 1st filter factor group accommodative using this reproduction digital data, and is outputted to the 1st variable filter, and the 2nd coefficient calculating means that updates the 2nd filter factor group accommodative using reproduction digital data, and is outputted to the 2nd variable filter.

[0022]The convergence time of the filter factor in the 1st coefficient calculating means constitutes so that it may become longer than the convergence time of the filter factor in the 2nd coefficient calculating means.
[0023]It constitutes so that renewal computation of the following coefficient may not be performed, until the convergence time of the filter factor in the 2nd coefficient calculating means passes, immediately after the 1st coefficient calculating means updates a filter factor.
[0024]It detects having been completed by each tap coefficient [in / in the 2nd coefficient calculating means / the 2nd variable filter], and a detection result is outputted, and it constitutes so that the 1st coefficient calculating means may perform renewal computation of the following coefficient in response to this detection result.
[0025]The 2nd coefficient calculating means detects variation per unit time of each tap coefficient, and it constitutes so that a detection result may be outputted, when variation of all the tap coefficients becomes smaller than a predetermined value.
[0026]An error detection decoder which detects an error of reproduction digital data and outputs an error flag is provided, and the 1st coefficient calculating means updates the 1st filter factor accommodative using an error flag outputted from this error detection decoder, and it constitutes so that it may output to the 1st variable filter.
[0027]The 1st variable filter constitutes so that only a frequency amplitude characteristic may be variable in a phase straight line.
[0028]The 1st variable filter and 2nd variable filter are constituted from the 1st transversal filter and 2nd transversal filter, respectively, A time delay between taps of the 1st transversal filter is changed with a time delay between taps of the 2nd transversal filter.
[0029]The time delay between the taps of the 1st transversal filter was set as Tb/2 (1 clock period of the digital signal into which Tb was inputted), and the time delay between the taps of

the 2nd transversal filter is set as Tb.

OPERATION

[Function]Therefore, since the automatic equalization circuit is divided into two steps, the state where many delay circuits carry out a multistage series connection, and frequency degradation occurs is avoidable. Until it distinguishs between the coefficient convergence time of two steps of each automatic equalization circuit or one automatic equalization circuit converges a filter factor, By suspending calculation of the filter factor of another automatic equalization circuit, the situation which two steps of automatic equalization circuits update a coefficient at the period, and a coefficient converges in the mistaken direction is avoided.
[0031]In one automatic equalization circuit, renewal of the coefficient is performed so that the number of the errors contained in reproduction digital data may decrease.
[0032]The flexibility of the frequency characteristic acquired in an equalizing circuit increases by constituting two steps of automatic equalization circuits from a transversal type variable filter, respectively, and changing the time delay between the taps of this filter in each transversal filter. Therefore, the total tap numbers which are needed in order to acquire the same equalization characteristic are reducible.

EXAMPLE

[Working example]The integration circuit 2 where an equalizing circuit in working example of this invention outputs an integral waveform of an input signal as shown in drawing 1, The 1st variable filter 3 that equalizes an input signal, and the 2nd variable filter 4 that equalizes an output signal of the 1st variable filter 3 further, The discrimination decision circuit 5 which discriminates digital data from an output signal of the 2nd variable filter 4, and is reproduced, ECC decoders 7 which perform error detection and an error correction of this reproduction digital data, The 1st coefficient calculation circuit 9 that calculates update values of a coefficient of the 1st variable filter 3 using an error number which ECC decoders 7 detected, It has the 2nd coefficient calculation circuit 6 that updates a coefficient of the 2nd variable filter 4 using an equalization signal of the 2nd variable filter 4, and reproduction digital data which the discrimination decision circuit 5 outputted.
[0034]The delay devices 10 and 11 with which the 1st variable filter 3 delays [$2 / T_1$=Tb/] an input signal (1 clock period of a digital signal into which Tb was inputted), It has the variable gain amplifiers 12 and 13 which amplify a signal with an amplification factor of a coefficient A updated by the 1st coefficient calculation circuit 9, and the adding machine 14 which adds an output signal of each variable gain amplifiers 12 and 13, and an output signal of the delay device 10, and is outputted to the 2nd variable filter 4.
[0035]The delay devices 20, 21, 22, and 23 with which only T_2= Tb delays the signal with which the 2nd variable filter 4 was outputted from the 1st variable filter 3, It has the variable gain amplifiers 24, 25, 26, 27, and 28 which amplify a signal with the amplification factor of the coefficient updated by the 2nd coefficient calculation circuit 6, respectively, and the adding

machines 29, 30, 31, and 32 which add the output signal of each variable gain amplifiers 24-28 one by one.

[0036]Next, operation of this equipment is explained.

[0037]First, a low-pass frequency component is compensated in the integration circuit 2, and the signal inputted from the input terminal 1 is inputted into the 1st variable filter 3.

[0038]In the 1st variable filter 3, the variable gain amplifier 12 amplifies the signal inputted from the integration circuit 2 with the amplification factor of a coefficient A (however, when a coefficient is a negative value). Moreover it reverses the polarity of an input signal, the variable gain amplifier 13 amplifies the signal for which only Tb ($=T_1x2$) was delayed with the delay devices 10 and 11 with the amplification factor of a coefficient A. The output signal of each variable gain amplifiers 12 and 13 is added with the adding machine 14 with the signal with which only T_1 was delayed by the delay device 10, and is outputted to the 2nd variable filter 4.

[0039]With the 2nd variable filter 4, the variable gain amplifier 24 amplifies the signal outputted from the 1st variable filter 3 with the amplification factor of coefficient-C_{-2}, and the variable gain amplifier 25 amplifies the signal for which only Tb was delayed with the delay device 20 with the amplification factor of coefficient-C_{-1}. Similarly, the variable gain amplifier 26 amplifies the output signal of the delay device 21 with the amplification factor of coefficient-C_0, and the variable gain amplifier 27 amplifies the output signal of the delay device 22 with the amplification factor of coefficient-C_{+1}, and the variable gain amplifier 28 amplifies the output signal of the delay device 23 with the amplification factor of coefficient-C_{+2}. Add the adding machine 29 and an output signal with the variable gain amplifiers 24 and 25 the adding machine 30, The adding machine 32 outputs the value adding the output signal of all the variable gain amplifiers 24, 25, 26, 27, and 28 eventually by adding the output signal of the variable gain amplifier 26 to the value further, and continuing it.

[0040]Equalization signal Y_{-1} outputted from the 2nd variable filter 4 is inputted into the discrimination decision circuit 5, and the discrimination decision circuit 5 discriminates digital data a_{-1} from equalization signal Y_{-1}, and outputs it as reproduction digital data. This discrimination decision circuit 5 is the same composition as what was explained by the conventional example.

[0041]Input equalization signal Y_{-1} and digital data a_{-1} into the 2nd coefficient calculation circuit 6, and the 2nd coefficient calculation circuit 6, Using this equalization signal Y_{-1} and digital data a_{-1}, the value of coefficient-C_{-2}, C_{-1}, C_0, C_{+1}, and C_{+2} is calculated, respectively, and it outputs to the variable gain amplifiers 24, 25, 26, 27, and 28 of the 2nd variable filter 4.

[0042]This composition and operation of the 2nd of the coefficient calculation circuit 6 are the same as what was previously explained by drawing 6, and only the point which the tap numbers of the filter only increased from 3 to 5 is different. Therefore, for every time Tb, the 2nd coefficient calculation circuit 6 follows the zero horsing method, and is the formulas 1, 2, and 3. -- Calculation is repeated and coefficient-C_{-2}, C_{-1}, C_0, C_{+1}, and C_{+2} are updated. As a result, these coefficients are recursively converged on the optimal coefficient value.

[0043]On the other hand, digital data a_{-1} outputted from the discrimination decision circuit 5 is inputted into ECC decoders 7. ECC decoders 7 perform processing of error detection or an error correction to this digital data, and output the digital data which corrected the error from the output terminal 8. At this time, ECC decoders 7 output the error flag which shows the existence of an error, or the thing (it is henceforth described as an error flag) which shows the frequency of error generating equivalent to this to the 1st coefficient calculation circuit 9 in processing of error detection or an error correction. Such ECC decoders are widely used in digital transmission

or digital recording now (for example, work besides Eto, the Digital Video record technology, Nikkan Kogyo Shimbun, 13 pages, 1990).
[0044]The 1st coefficient calculation circuit 9 that this error flag inputs, The error frequency counters 91 which count the number of the error flags outputted from ECC decoders 7 as shown in drawing 2 (a), The coefficient generator 96 which outputs a different coefficient for every period to the 1st variable filter 3, The memories 93 and 94 which memorize the count number of the error flag of a different period, respectively, It has the change-over switch 92 which switches the memories 93 and 94 which are mistaken for every period of the and connect with the frequency counters 91, and the judging device 95 which judges a suitable coefficient value based on the value memorized by the memories 93 and 94.
[0045]In order that the coefficient generator 96 of this coefficient calculation circuit 9 may control that operation timing to the error frequency counters 91, the change-over switch 92, the memories 93 and 94, and the judging device 95, As shown in drawing 2 (b), the control signal 81 reversed to predetermined every periodic **T is outputted through the signal wire 98, and the value (82 of drawing 2 (b)) of a coefficient A is changed and outputted to the 1st variable filter 3 according to this cycle. That is, A_1 is outputted to the cycle 84 as a coefficient, and A_2 in which only predetermined value **a is smaller than A_1 is outputted to the cycle 85 as a coefficient.
[0046]The error frequency counters 91 reset a counter value, whenever the control signal to input changes, and they calculate the number of the error flags inputted from ECC decoders 7 during the **T. When this counter value is shown in 83 of drawing 2 (b) and the 1st variable filter 3 performs equalization by coefficient A_1, the error flag of E_1 occurs between time **T, When the 1st variable filter 3 performs equalization by coefficient A_2, it is shown that the error flag of E_2 occurred.
[0047]Number of error flags E_2 which number of error flags E_1 which the error frequency counters 91 counted at the last of the period 84 was stored in the memory 93 via the change-over switch 92, and was counted at the last of the period 85 is stored in the memory 94 via the change-over switch 92. The judging device 95 compares the number of error flags stored in this memory 93 and memory 94, judges coefficient value A_2 corresponding to E_2 with that small value to be a thing near optimal coefficient value, and outputs a decided result to the coefficient generator 96.
[0048]In the 1st variable filter 3, the same coefficient A outputted to the variable gain amplifiers 12 and 13 from the coefficient generator 96 is given. At this time, the transfer characteristic H (f) of the 1st variable filter 3 is $H(f) = Z^{-1} + A(Z^0 + Z^{-2})$.
$= Z^{-1}\{1+2A\text{-}\cos(2\pi\text{-}T_1/f)\}$ (formula 4)
(However, f:frequency, $Z^{-1}=\exp(-j\omega T_1)$, omega: Angular frequency)
It becomes. Therefore, a phase characteristic serves as a straight line and only a frequency amplitude characteristic changes to change of a coefficient A. At this time, a coefficient A and the error frequency which ECC decoders 7 detect serve as a relation as shown in drawing 2 (C).
[0049]Therefore, when the coefficient generator 96 receives the decided result that the direction of coefficient value A_2 ($<A_1$) has few error flags from the judging device 95, When the coefficient value in which only further predetermined value **a is smaller than coefficient value A_2 is outputted to the next period and the decided result that the direction of coefficient value A_1 has few error flags is received conversely, It is completed as an optimum value by the coefficient A by outputting the coefficient value in which only **a is still larger to the next period, and repeating such operation rather than coefficient value A_1, in it.
[0050]In this way, exact equalization becomes possible when completed as an optimum value by

both the coefficient of the 1st variable filter 3 of this equalizing circuit, and the coefficient of the 2nd variable filter 4.

[0051]However, in this circuit, if a coefficient A changes, the frequency spectra of the signal outputted from the 1st variable filter 3 change, therefore the characteristic of the 2nd variable filter 4 will also be combined and will change to it. Therefore, when it mistakes in the stage in the middle of both the coefficient of the 1st variable filter 3 and the coefficient of the 2nd variable filter changing and frequency is detected, a possibility that the relation shown in drawing 2 (C) may stop realizing is between a coefficient A and the error frequency which ECC decoders detect.

[0052]In order to avoid this, when setting time until it is recursively completed as an optimum value by each coefficient of the 2nd variable filter 4 to **Tc as the 1st method, there is the method of setting it as a sufficiently long cycle to such an extent that the influence of **Tc can disregard predetermined periodic **T in drawing 2 (b).

[0053]In the error frequency counters 91, the 2nd methods include the method of making it not calculate an error flag after being reset until time **Tc passes.

[0054]As the 3rd method, it detects having been completed by each coefficient of the 2nd variable filter 4 in the 2nd coefficient calculation circuit 6, A detection result is mistaken, it transmits to the frequency counters 91, and there is the method of constituting so that calculation of an error flag may be started after the error frequency counters 91 check convergence of the 2nd variable filter 4. In this case, in order to detect having been completed by each coefficient of the 2nd variable filter 4 in the 2nd coefficient calculation circuit 6, When the variation between time Tb of each coefficient is detected and the variation of all the coefficients becomes smaller than a predetermined value, a detection result is made to output as that which the coefficient in the 2nd variable filter 4 converged.

[0055]By taking such a means, the convergence time of the 1st variable filter 3 becomes longer than the convergence time of the 2nd variable filter 4, and immediately after changing a coefficient, the 1st variable filter 3 does not perform renewal computation of the following coefficient until the convergence time of the 2nd variable filter 4 passes. As a result, in this equalizing circuit, the 1st variable filter 3 and 2nd variable filter 4 repeat convergence by turns, and it is eventually completed as an optimum value by both the coefficients of both filters.

[0056]Thus, making convergence time of the 1st variable filter 3 longer than the convergence time of the 2nd variable filter 4, Conversely, if it sees, in the equalizing circuit of working example, it will become possible to use the circuit which operates to the 1st coefficient calculation circuit 9 at a low speed as compared with the 2nd coefficient calculation circuit 6, and the part and realization will become easy.

[0057]Time delay T_1 [in / in this equalizing circuit / the delay devices 10 and 11 of the 1st variable filter 3] (=Tb/2), By changing time delay T_2 (=Tb) in the delay devices 20, 21, 22, and 23 of the 2nd variable filter 4, as shown below, it makes it possible to reduce the total of the required tap numbers in the 1st and 2nd variable filters.

[0058]Drawing 3 shows the frequency characteristic of the 1st variable filter 3. The dotted line in a figure is a case where time delay T_1 of the delay devices 10 and 11 is set as Tb/2.

A solid line is a case where time delay T_1 of the delay devices 10 and 11 is set as T_1=Tb like the delay device of the 2nd variable filter 4.

As a dotted line shows, when time delay T_1 are Tb/2, the peak of a frequency characteristic appears in 1/Tb. On the other hand, when time delay T_1 is Tb, as a solid line shows, the peak of a frequency characteristic appears in 1/(2Tb). The frequency characteristic in the conventional

equalizing circuit of drawing 4 which has a delay device of time delay Tb, and the 2nd variable filter 4 of this working example also becomes being the same as that of this solid line, and shows symmetry type by the low frequency wave and high frequency side by making peak frequency 1/(2Tb) into the point of symmetry.

[0059]Therefore, in time delay T_1 of the delay devices 10 and 11 of the 1st variable filter 3 being the same as time delay Tb of the delay devices 20-23 of the 2nd variable filter 4, even if it combines those filters, only the frequency characteristic of a tendency shown in a solid line can be acquired.

[0060]on the other hand, when a time delay in the 1st variable filter 3 is changed with a time delay of the 2nd variable filter 4, various frequency characteristics of a high region zone especially constructed in 1/[from frequency 1/(2Tb)] Tb can be boiled and changed by combining those filters. That is, by changing a time delay of the 1st variable filter 3, and a time delay of the 2nd variable filter 4, flexibility of an equalization characteristic can be increased, therefore a desired equalization characteristic can be acquired by a small number of taps.

[0061]On the other hand, when tap numbers of the conventional equalizing circuit of drawing 4 tend to be increased simply and it is going to acquire a comparable equalization characteristic, very many tap numbers are needed. In order that it will be necessary to combine with an increase in tap numbers and to enlarge a scale of the coefficient calculation circuit 56 in this case and and a delay circuit may carry out many series connections, degradation of a frequency characteristic occurs.

[0062]In the equalizing circuit of working example, frequency degradation by the multistage series connection of a delay circuit is avoided by dividing the variable filter of an automatic equalization circuit into two steps of the 1st variable filter 3 and the 2nd variable filter 4.

[0063]When the equalizing circuit of working example provides a difference in the convergence time of the coefficient in two steps of automatic equalization circuits, it avoids that two steps of automatic equalization circuits have an adverse effect on convergence of a coefficient mutually.

[0064]The 1st variable filter 3 of this equalizing circuit has a linear phase characteristic, and it is constituted so that only a frequency amplitude characteristic may change, when a coefficient A is changed. Based on the error flag from ECC decoders, the calculation circuit which updates this coefficient A updates a coefficient so that error generating of a reproduction digital signal may always serve as the minimum. The calculation circuit of this coefficient can simplify that composition compared with the conventional coefficient calculation circuit.

[0065]By constituting two steps of automatic equalization circuits using a both transversal type variable filter, and changing the time delay between two taps of a transversal filter in this equalizing circuit, respectively, Total tap numbers required in order to acquire the same equalization characteristic are reducible.

[0066]In the equalizing circuit of working example, although the tap numbers of the 2nd variable filter 4 were set to 5, even if it changes these tap numbers, the same effect can be acquired. Although the time delay in the 1st variable filter 3 is set as T_1=Tb/2, this time delay can be made into any value. Although the tap numbers of the 1st variable filter 3 were set to 3 and it was considered as the one number of the coefficients to change, it is not necessarily restricted to this and tap numbers and the number of coefficients to change may be made still larger.

[0067]Although working example described the equalizing circuit which used the zero horsing method, the thing using other algorithms is also the same. This equalizing circuit can use not only reproduction of magnetic recording but optical recording etc. for reproduction of the data recorded by other recording principles, or can also be used as an equalizing circuit of the digital

transmission instead of record.

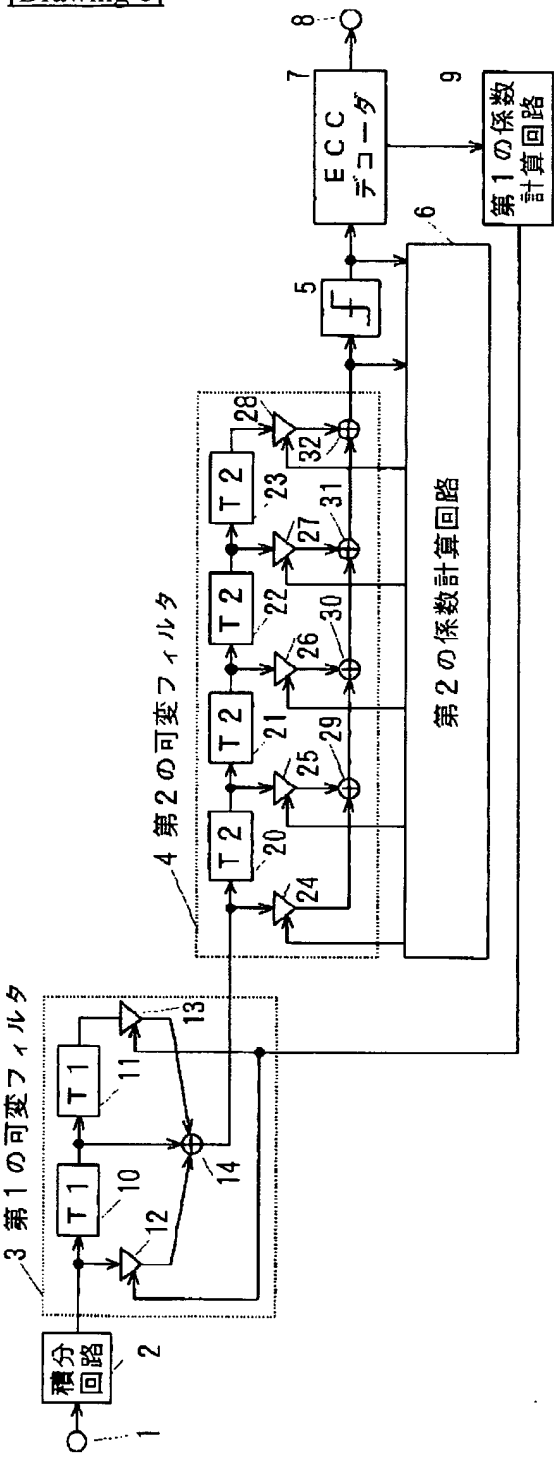
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]The block diagram showing the composition of the equalizing circuit in working example of this invention,
[Drawing 2]The block diagram (a) showing the 1st coefficient calculation circuit of the equalizing circuit of working example, the figure (b) showing the signal wave form of each part of this 1st coefficient calculation circuit, the figure (c) showing the relation between the coefficient A which the 1st coefficient calculation circuit outputs, and the error frequency which ECC decoders detect,
[Drawing 3]The figure showing the change in the frequency characteristic of the 1st variable filter when the time delay of a delay device is changed,
[Drawing 4]The block diagram showing the composition of the conventional equalizing circuit,
[Drawing 5]The signal spectrum figure of the signal outputted from a playback head,
[Drawing 6]It is a block diagram showing the coefficient calculation circuit in the conventional equalizing circuit.
[Explanations of letters or numerals]
1 Input terminal
2 and 45 Integration circuit
3 The 1st variable filter
4 The 2nd variable filter
5 and 55 Discrimination decision circuit
6 The 2nd coefficient calculation circuit
7 ECC decoders
8, 54, 57, and 97 Output terminal
9 The 1st coefficient calculation circuit
10, 11, 20-23 Delay device
12, 13, 24-28 A variable gain amplifier
14, 29-32, and 53 An adding machine
41 Magnetic tape
42 A playback head
43 An equalizing circuit
44, 47, 61, 62, and 90 An input terminal
46 A transversal filter
48, 49, 64, 68, and 69 A delay circuit
50-52 A variable gain amplifier
56 A coefficient calculation circuit
63 A subtractor
65-67 A calculation circuit
82 A coefficient A
83 An output signal from the error frequency counters 91
91 Error frequency counters

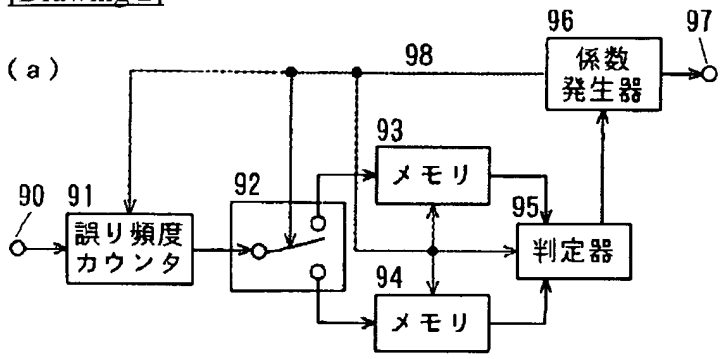
92 A change-over switch
93 and 94 A memory
95 A judging device
96 A coefficient generator

DRAWINGS

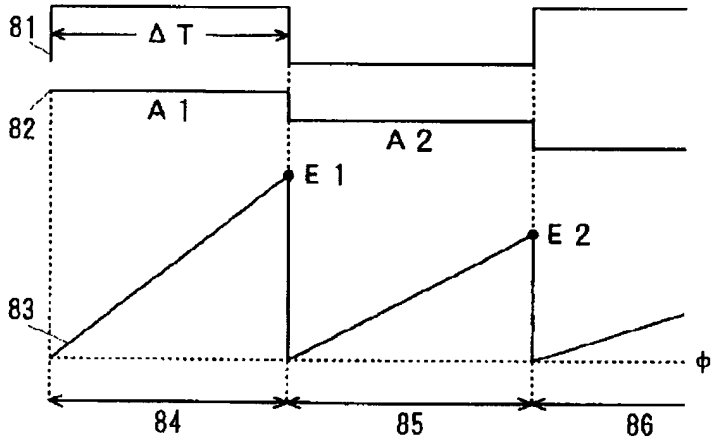
[Drawing 1]



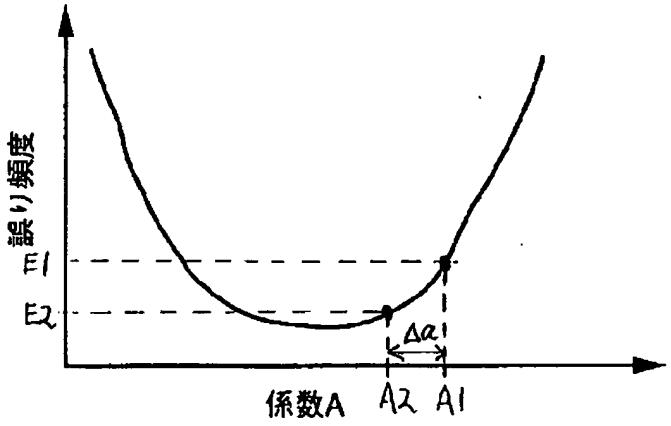
[Drawing 2]


(a)
96
97
98
係数
発生器
93
メモリ
90
91
92
95
誤り頻度
カウンタ
判定器
94
メモリ

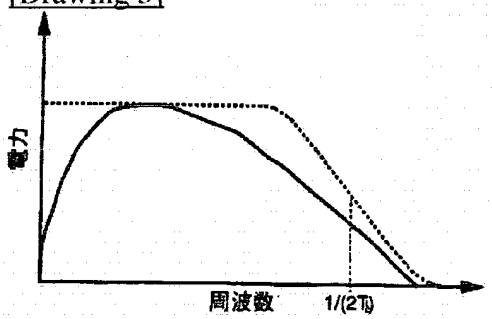
(b)


81
ΔT
A 1
82
A 2
E 1
E 2
83
φ
84
85
86

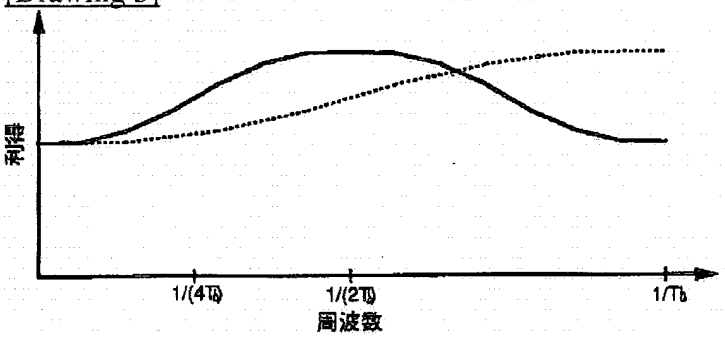
(c)


誤り頻度
E1
E2
Δa1
係数A
A2
A1

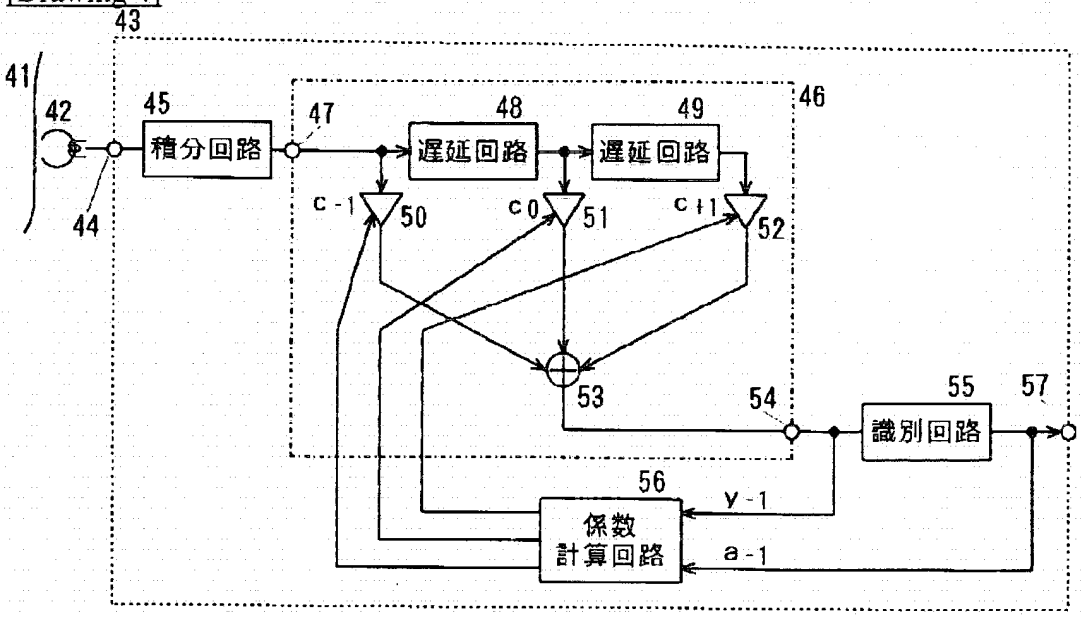
[Drawing 5]



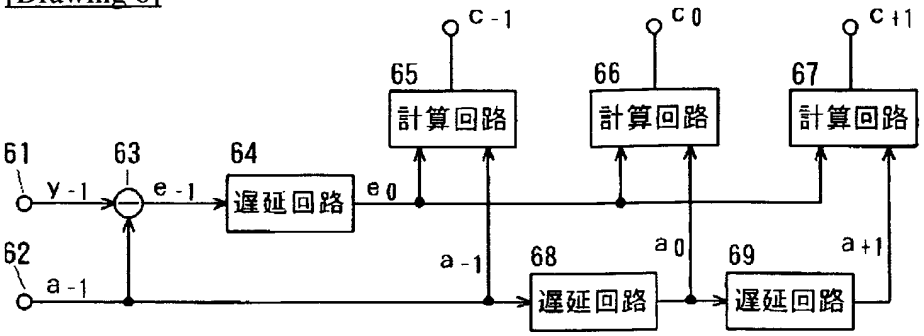
[Drawing 3]



[Drawing 4]



[Drawing 6]


c -1
c 0
c +1
65
66
67
計算回路
計算回路
計算回路
61
63
64
y -1
e -1
遅延回路
e 0
62
a -1
a -1
68
a 0
69
a +1
遅延回路
遅延回路

ENGLISH TRANSLATION OF POINTED PART OF
Japanese Patent Application Publication JP-A-H08-161832A

[0025] Further, the second coefficient calculation means detects a change amount of each tap coefficient per unit time, and outputs the detection result when the change amounts of all tap coefficients become smaller than a predetermined value.

[0054] Further, as the third method, there is a method of detecting, in the second coefficient calculation circuit 6, that each coefficient of the second variable filter 4 converges, transferring the detection result to the error frequency counter 91, and starting count of error flags after the error frequency counter 91 confirms convergence of the second variable filter 4. In this case, in order to detect that each coefficient of the second variable filter 4 has converged, the second coefficient calculation circuit 6 detects a change amount of each coefficient during a time Tb. When the change amounts of all coefficients become smaller than a predetermined value, it is assumed that each coefficient of the second variable filter 4 has converged, and the detection result is outputted.

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(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
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5/09	３２１　Ａ	7520－5D		
20/18	５７０　Ｄ	8940－5D		

審査請求　未請求　請求項の数９　ＦＤ　（全 10 頁）

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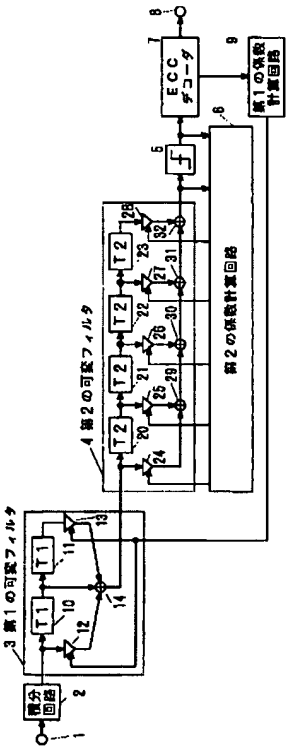
(54)【発明の名称】　等化回路

(57)【要約】

【目的】　実現し易く、少ないハードウエアで、正確な等化の行なえる等化器を提供する。

【構成】　自動等化回路の可変フィルタを第１可変フィルタ３と第２可変フィルタ４の２段に分離し、遅延回路の多段直列接続による周波数劣化を避ける。また、２段の自動等化回路の係数収束時間に差をつけることにより、２段の自動等化回路がお互いに係数の収束に悪影響を与え合うことを避ける。第１可変フィルタ３は、位相直線で、１つの係数Ａにより周波数振幅特性のみが可変する。この可変フィルタ３の係数Ａは、ＥＣＣデコーダ７からのエラーフラグ数が極小となるように更新される。２つのトランスバーサルフィルタ３、４の、タップ間の遅延時間を変えることで、同じ等化特性を得るために必要なトータルのタップ数を削減することができる。



【特許請求の範囲】

【請求項1】　伝送または再生されたディジタル信号をディジタルフィルタを用いて等化する等化回路において、

入力信号を、外部から入力される第1のフィルタ係数群に従って等化し、第1の等化信号を出力する第1の可変フィルタと、

前記第1の等化信号を、外部から入力される第2のフィルタ係数群に従って等化し、第2の等化信号を出力する第2の可変フィルタと、

前記第2の等化信号を識別し、再生ディジタルデータを出力する識別手段と、

前記再生ディジタルデータを用いて、第1のフィルタ係数群を適応的に更新し、第1の可変フィルタに出力する第1の係数計算手段と、

前記再生ディジタルデータを用いて、第2のフィルタ係数群を適応的に更新し、第2の可変フィルタに出力する第2の係数計算手段と、を具備することを特徴とする等化回路。

【請求項2】　前記第1の係数計算手段におけるフィルタ係数の収束時間が、前記第2の係数計算手段におけるフィルタ係数の収束時間よりも長いことを特徴とする請求項1に記載の等化回路。

【請求項3】　前記第1の係数計算手段が、フィルタ係数の更新を行なった直後に、前記第2の係数計算手段におけるフィルタ係数の収束時間が経過するまで、次の係数の更新演算を行なわないことを特徴とする請求項1に記載の等化回路。

【請求項4】　前記第2の係数計算手段が、前記第2の可変フィルタにおける各タップ係数が収束したことを検出して検出結果を出力し、前記第1の係数計算手段が、前記検出結果を受けて次の係数の更新演算を行なうことを特徴とする請求項1に記載の等化回路。

【請求項5】　前記第2の係数計算手段が、前記各タップ係数の単位時間当たりの変化量を検出し、全てのタップ係数の変化量が所定の値より小さくなったときに前記検出結果を出力することを特徴とする請求項4に記載の等化回路。

【請求項6】　前記再生ディジタルデータの誤りを検出し、エラーフラグを出力する誤り検出デコーダを設け、前記第1の係数計算手段が、前記誤り検出デコーダから出力されたエラーフラグを用いて、前記第1のフィルタ係数を適応的に更新し、前記第1の可変フィルタに出力することを特徴とする請求項1乃至5に記載の等化回路。

【請求項7】　前記第1の可変フィルタが、位相直線で周波数振幅特性のみが可変であることを特徴とする請求項1乃至6に記載の等化回路。

【請求項8】　前記第1の可変フィルタと第2の可変フィルタとが、それぞれ第1のトランスバーサルフィルタと第2のトランスバーサルフィルタとから成り、前記第1のトランスバーサルフィルタのタップ間の遅延時間が、第2のトランスバーサルフィルタのタップ間の遅延時間と異なることを特徴とする請求項1乃至7に記載の等化回路。

【請求項9】　前記第1のトランスバーサルフィルタのタップ間の遅延時間をTb／2（Tbは、入力されたディジタル信号の1クロック周期）に設定し、前記第2のトランスバーサルフィルタのタップ間の遅延時間をTbに設定したことを特徴とする請求項8に記載の等化回路。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、ディジタル情報が伝送や記録装置からの再生の際に受ける劣化を自動的に補償する等化回路に関し、特に、小規模のハードウエアで正確な等化が実現できるようにしたものである。

【0002】

【従来の技術】従来、ディジタル磁気記録再生装置で再生された信号に対して、再生信号の信頼性を高めるために、等化回路を用いてその周波数特性を自動等化することが行なわれている（例えば、三田、井手、稲垣：ディジタルVTR用簡易自動等化器、テレビジョン学会技術報告、13巻、59号、7～12頁、VIR'89－20、1989年）。

【0003】この等化回路は、図4に示すように、入力する再生信号の積分波形を出力する積分回路45と、入力信号に等化処理を施すトランスバーサルフィルタ46と、トランスバーサルフィルタ46の等化出力からディジタルデータを識別して再生する識別回路55と、トランスバーサルフィルタ46の等化出力と識別回路55の再生ディジタルデータとからトランスバーサルフィルタ46における係数の更新値を計算する係数計算回路56とから成り、トランスバーサルフィルタ46は、入力信号をディジタル信号の1クロック周期Tb分ずつ遅延させる遅延回路48、49と、更新された係数の増幅率で信号を増幅する可変利得増幅回路50、51、52と、各可変利得増幅回路50～52の出力を加算し等化出力として出力する加算器53とを備えている。

【0004】この等化回路43の入力端子44には、磁気テープ41に記録されたディジタル信号を再生した再生ヘッド42の再生出力が入力する。

【0005】この再生ヘッド42から出力される信号の信号スペクトラムは、図5に実線で示すように、低域周波数成分が微分特性を示している。即ち、磁気記録再生系では、直流成分は再生されず、周波数が低いほど再生信号に含まれる電力が少なくなる。また、高域周波数成分は、ギャップ損失、スペーシング損失などの各種損失により、再生される電力が減ってくる。

【0006】このため、再生信号を高い信頼性でディジ

タル符号に戻すためには、正確な等化を行なうことが必要となる。このことは、再生信号の周波数特性を、いわゆるロールオフ特性（一例を図５に破線で示した）に近づけるように等化することで実現される。

【０００７】図４に戻って、入力端子44に入力した信号は、積分回路45で低域周波数成分が補償され、トランスバーサルフィルタ46に入力する。

【０００８】トランスバーサルフィルタ46では、可変利得増幅回路50が入力端子47に入力した信号を係数C_{-1}の増幅率で増幅し（ただし、係数が負の値の時は、入力信号の極性を反転させるものとする）、可変利得増幅回路51が、遅延回路48で１クロック周期Ｔｂだけ遅延された入力信号を係数C_0の増幅率で増幅し、また、可変利得増幅回路52が、遅延回路49でさらに１クロック周期Ｔｂだけ遅延された入力信号を係数C_{+1}の増幅率で増幅する。各可変利得増幅回路50～52の出力信号は加算器53に入力し、加算器53はそれらの加算値である等化信号Y_{-1}を出力端子54より出力する。

【０００９】トランスバーサルフィルタ46から出力された等化信号Y_{-1}は、識別回路55と係数計算回路56とに入力する。識別回路55は、等化信号Y_{-1}からディジタルデータa_{-1}を識別し、出力端子57に出力する。この識別回路55は、例えばコンパレータを用いて等化信号Y_{-1}を所定の基準レベルと比較することにより容易に実現することができる。

【００１０】ディジタルデータa_{-1}は係数計算回路56にも入力し、係数計算回路56は、記録データと等化信号Y_{-1}との誤差の近似値として、ディジタルデータa_{-1}と等化信号Y_{-1}との誤差を用いて、この誤差が収斂するように係数C_{-1}、C_0、C_{+1}の更新値を計算し、トランスバーサルフィルタ46の各可変利得増幅回路50～52に出力する。

【００１１】この係数計算回路56は、図６に示すように、等化信号Y_{-1}の入力する入力端子61と、ディジタルデータa_{-1}の入力する入力端子62と、Y_{-1}とa_{-1}との誤差e_{-1}を出力する減算器63と、この誤差を周期Ｔｂだけ遅延させる遅延回路64と、ディジタルデータa_{-1}を周期Ｔｂだけ遅延させる遅延回路68、69と、遅延させた誤差e_0とa_{-1}とからC_{-1}の更新値を計算する計算回路65と、誤差e_0と遅延回路68の出力a_0とからC_0の更新値を計算する計算回路66と、誤差e_0と遅延回路69の出力a_{+1}とからC_{+1}の更新値を計算する計算回路67とから成る。

【００１２】入力端子61に入力した等化信号Y_{-1}と入力端子62に入力したディジタルデータa_{-1}とは、減算器63に与えられ、減算器63は、信号Y_{-1}から信号a_{-1}を減算して誤差$e_{-1}=Y_{-1}-a_{-1}$を出力する。遅延回路64は、誤差e_{-1}を周期Ｔｂの時間だけ遅延させる。この遅延した信号を誤差e_0とする。遅延回路64は、誤差e_0を計算回路65、66、67にそれぞれ与える。

【００１３】一方、入力端子62から入力したディジタルデータa_{-1}は、計算回路65及び遅延回路68に入力する。遅延回路68は、この信号を１Ｔｂ遅延させてa_0として出力し、この出力が入力した遅延回路69は、さらに１Ｔｂ遅延させてa_{+1}として出力する。従って、ディジタルデータa_{-1}、a_0、a_{+1}の遅延量は、それぞれ０Ｔｂ、１Ｔｂ、２Ｔｂである。これらの信号a_{-1}、a_0、a_{+1}は、それぞれ計算回路65、66、67に与えられる。

【００１４】計算回路65、66、67は、時間Ｔｂ毎に繰り返し次のような計算を行なう。ある時刻ｉに、計算回路65、66、67にそれぞれ信号a_{-1}、a_0、a_{+1}及び誤差e_0が入力したものとする。このとき、計算回路65、66、67は、時刻ｉにおけるトランスバーサルフィルタ46の係数$C_{-1}(i)$、$C_0(i)$、$C_{+1}(i)$を用いて、時間Ｔｂだけ経過した後の時刻（ｉ＋１）におけるトランスバーサルフィルタ46の係数$C_{-1}(i+1)$、$C_0(i+1)$、$C_{+1}(i+1)$を次の３つの式によって計算する。

【００１５】

$$C_{-1}(i+1)=C_{-1}(i)-\alpha\cdot e_0\cdot a_{-1} \quad (式1)$$

$$C_0(i+1)=C_0(i)-\alpha\cdot e_0\cdot a_0 \quad (式2)$$

$$C_{+1}(i+1)=C_{+1}(i)-\alpha\cdot e_0\cdot a_{+1} \quad (式3)$$

ただし、ここでαは係数の値の収束の速度を決定する定数で、収束係数と呼ばれる。上記の計算を、時間Ｔｂ毎に繰り返し、トランスバーサルフィルタ46の係数C_{-1}、C_0、C_{+1}を更新する。

【００１６】このようなフィルタの係数の計算は、ゼロ・フォーシング法と呼ばれる（例えば、宮川他　著、電子通信学会編：ディジタル信号処理、電子通信学会、２３３頁、１９８１年（９版））。この更新により係数C_{-1}、C_0、C_{+1}は、再帰的に、最適値に収束する。

【００１７】この自動等化によって再生信号の信頼性が向上し、磁気テープ41に記録されたデータの忠実な再生が可能になる。

【００１８】【発明が解決しようとする課題】しかし、従来の自動等化回路は、複雑なハードウエアが必要である。即ち、この等化回路で正確な等化を行なおうとすると、トランスバーサルフィルタ46のタップ数を多くしなければならないが、しかし、タップ数が増えれば増えるほど、ハードウエアの実現は困難になる。

【００１９】また、近年、高解像度の映像信号をディジタル伝送・記録することが必要になってきているが、このような高データレートのディジタル信号を伝送・記録するためには、等化回路においても広帯域の信号を取り扱わなければならない。しかし、信号帯域が広がると、全帯域について正確に同じ時間だけ遅延させる遅延回路を構成することが難しい。また、遅延回路を多段に直列

接続した場合には、遅延する信号の周波数特性の劣化を招き易い。これらの理由により、従来、高データレートのディジタル信号を正確に等化し得る等化回路を構成することが非常に困難であった。

【００２０】本発明は、こうした従来の問題点を解決するものであり、高データレートのディジタル信号についても、小規模で実現の容易なハードウエアによって正確に自動等化することができる等化回路を提供することを目的としている。

【００２１】

【課題を解決するための手段】そこで、本発明では、伝送または再生されたディジタル信号をディジタルフィルタを用いて等化する等化回路において、入力信号を外部から入力される第１のフィルタ係数群に従って等化し第１の等化信号を出力する第１の可変フィルタと、この第１の等化信号を外部から入力される第２のフィルタ係数群に従って等化し第２の等化信号を出力する第２の可変フィルタと、この第２の等化信号を識別して再生ディジタルデータを出力する識別手段と、この再生ディジタルデータを用いて第１のフィルタ係数群を適応的に更新し、第１の可変フィルタに出力する第１の係数計算手段と、再生ディジタルデータを用いて第２のフィルタ係数群を適応的に更新し、第２の可変フィルタに出力する第２の係数計算手段とを設けている。

【００２２】また、第１の係数計算手段におけるフィルタ係数の収束時間が、第２の係数計算手段におけるフィルタ係数の収束時間よりも長くなるように構成している。

【００２３】また、第１の係数計算手段が、フィルタ係数の更新を行なった直後に、第２の係数計算手段におけるフィルタ係数の収束時間が経過するまで、次の係数の更新演算を行なわないように構成している。

【００２４】また、第２の係数計算手段が第２の可変フィルタにおける各タップ係数が収束したことを検出して検出結果を出力し、第１の係数計算手段がこの検出結果を受けて次の係数の更新演算を行なうように構成している。

【００２５】また、第２の係数計算手段が各タップ係数の単位時間当たりの変化量を検出し、全てのタップ係数の変化量が所定の値より小さくなったときに検出結果を出力するように構成している。

【００２６】また、再生ディジタルデータの誤りを検出しエラーフラグを出力する誤り検出デコーダを設け、第１の係数計算手段が、この誤り検出デコーダから出力されたエラーフラグを用いて第１のフィルタ係数を適応的に更新し、第１の可変フィルタに出力するように構成している。

【００２７】また、第１の可変フィルタが、位相直線で周波数振幅特性のみが可変であるように構成している。

【００２８】また、第１の可変フィルタと第２の可変フィルタとをそれぞれ第１のトランスバーサルフィルタと第２のトランスバーサルフィルタとで構成し、第１のトランスバーサルフィルタのタップ間の遅延時間を第２のトランスバーサルフィルタのタップ間の遅延時間と異ならせている。

【００２９】さらに、第１のトランスバーサルフィルタのタップ間の遅延時間をＴｂ／２（Ｔｂは入力されたディジタル信号の１クロック周期）に設定し、第２のトランスバーサルフィルタのタップ間の遅延時間をＴｂに設定している。

【００３０】

【作用】そのため、自動等化回路を２段に分離しているので、多数の遅延回路が多段直列接続して周波数劣化が発生する状態を避けることができる。また、２段の各自動等化回路の係数収束時間に差を付けたり、一方の自動等化回路がフィルタ係数を収束するまで、もう一方の自動等化回路のフィルタ係数の計算を停止することによって、２段の自動等化回路が同時期に係数を更新し、誤った方向に係数が収束する事態を避けている。

【００３１】また、一方の自動等化回路では、再生ディジタルデータに含まれる誤りの数が減少するように、その係数の更新が行なわれる。

【００３２】また、２段の自動等化回路をそれぞれトランスバーサル型の可変フィルタで構成し、このフィルタのタップ間の遅延時間をそれぞれのトランスバーサルフィルタにおいて違えることによって、等化回路で得られる周波数特性の自由度が増加する。そのため、同じ等化特性を得るために必要となるトータルのタップ数を削減することができる。

【００３３】

【実施例】本発明の実施例における等化回路は、図１に示すように、入力信号の積分波形を出力する積分回路２と、入力信号を等化する第１の可変フィルタ３と、第１の可変フィルタ３の出力信号をさらに等化する第２の可変フィルタ４と、第２の可変フィルタ４の出力信号からディジタルデータを識別して再生する識別回路５と、この再生ディジタルデータの誤り検出・誤り訂正を行なうＥＣＣデコーダ７と、ＥＣＣデコーダ７の検出したエラー数を用いて第１の可変フィルタ３の係数の更新値を計算する第１の係数計算回路９と、第２の可変フィルタ４の等化信号と識別回路５の出力した再生ディジタルデータとを用いて第２の可変フィルタ４の係数を更新する第２の係数計算回路６とを備えている。

【００３４】また、第１の可変フィルタ３は、入力信号をT_1＝Ｔｂ／２だけ遅延させる（Ｔｂは入力されたディジタル信号の１クロック周期）遅延器10、11と、第１の係数計算回路９によって更新される係数Ａの増幅率で信号を増幅する可変利得増幅回路12、13と、各可変利得増幅回路12、13の出力信号及び遅延器10の出力信号を加算して第２の可変フィルタ４に出力する加算器14とを備

えている。

【００３５】また、第２の可変フィルタ４は、第１の可変フィルタ３から出力された信号をT_2 ＝Ｔｂだけ遅延させる遅延器20、21、22、23と、第２の係数計算回路６によってそれぞれ更新される係数の増幅率で信号を増幅する可変利得増幅回路24、25、26、27、28と、各可変利得増幅回路24～28の出力信号を順次加算する加算器29、30、31、32とを備えている。

【００３６】次に、この装置の動作について説明する。

【００３７】まず、入力端子１から入力した信号は、積分回路２で低域周波数成分が補償され、第１の可変フィルタ３に入力する。

【００３８】第１の可変フィルタ３では、可変利得増幅回路12が積分回路２から入力した信号を係数Ａの増幅率で増幅し（ただし、係数が負の値の時は、入力信号の極性を反転させる）、また、可変利得増幅回路13が遅延器10及び11によりＴｂ（＝T_1×２）だけ遅延された信号を係数Ａの増幅率で増幅する。各可変利得増幅回路12、13の出力信号は、遅延器10でT_1 だけ遅延された信号とともに加算器14で加算され、第２の可変フィルタ４に出力される。

【００３９】第２の可変フィルタ４では、可変利得増幅回路24が、第１の可変フィルタ３から出力された信号を係数C_{-2}の増幅率で増幅し、可変利得増幅回路25が、遅延器20によりＴｂだけ遅延された信号を係数C_{-1}の増幅率で増幅する。同様に、可変利得増幅回路26は遅延器21の出力信号を係数C_0 の増幅率で増幅し、可変利得増幅回路27は遅延器22の出力信号を係数C_{+1}の増幅率で増幅し、また、可変利得増幅回路28は遅延器23の出力信号を係数C_{+2}の増幅率で増幅する。また、加算器29は可変利得増幅回路24と25との出力信号を加算し、加算器30は、その値にさらに可変利得増幅回路26の出力信号を加算し、それを続けることによって、最終的に加算器32は、全ての可変利得増幅回路24、25、26、27、28の出力信号を加算した値を出力する。

【００４０】第２の可変フィルタ４から出力された等化信号Y_{-1}は識別回路５に入力し、識別回路５は、等化信号Y_{-1}からディジタルデータa_{-1}を識別して再生ディジタルデータとして出力する。この識別回路５は、従来例で説明したものと同じ構成である。

【００４１】等化信号Y_{-1}及びディジタルデータa_{-1}は第２の係数計算回路６に入力し、第２の係数計算回路６は、この等化信号Y_{-1}とディジタルデータa_{-1}とを用いて、係数C_{-2}、C_{-1}、C_0 、C_{+1}、C_{+2}の値をそれぞれ演算し、第２の可変フィルタ４の可変利得増幅回路24、25、26、27、28に出力する。

【００４２】この第２の係数計算回路６の構成及び動作は、先に図６で説明したものと同じであり、単にフィルタのタップ数が３から５に増加した点だけが違っている。従って、第２の係数計算回路６は、時間Ｔｂごとに、ゼロ・フォーシング法に則って、式１、２、３‥の計算を繰り返し、係数C_{-2}、C_{-1}、C_0 、C_{+1}、C_{+2}を更新する。その結果、これらの係数は再帰的に、最適な係数値に収束する。

【００４３】一方、識別回路５から出力されたディジタルデータa_{-1}はＥＣＣデコーダ７に入力する。ＥＣＣデコーダ７は、このディジタルデータに誤り検出や誤り訂正の処理を行ない、誤りを訂正したディジタルデータを出力端子８より出力する。このとき、ＥＣＣデコーダ７は、誤り検出や誤り訂正の処理において、誤りの有無を示すエラーフラグ、またはこれに相当する誤り発生の頻度を示すもの（以降、エラーフラグと記す）を第１の係数計算回路９に出力する。このようなＥＣＣデコーダは、現在、ディジタル伝送やディジタル記録において広く用いられている（例えば、江藤他　著、ディジタルビデオ記録技術、日刊工業新聞社、１３頁、１９９０年）。

【００４４】このエラーフラグが入力する第１の係数計算回路９は、図２（ａ）に示すように、ＥＣＣデコーダ７から出力されたエラーフラグの数をカウントする誤り頻度カウンタ91と、第１の可変フィルタ３に期間ごとに異なる係数を出力する係数発生器96と、異なる期間のエラーフラグのカウント数をそれぞれ記憶するメモリ93と94と、その期間ごとに誤り頻度カウンタ91に接続するメモリ93、94を切換える切換スイッチ92と、メモリ93、94に記憶された値に基づいて適切な係数値を判定する判定器95とを備えている。

【００４５】この係数計算回路９の係数発生器96は、誤り頻度カウンタ91、切換スイッチ92、メモリ93、94、及び判定器95に対して、その動作タイミングを制御するため、図２（ｂ）に示すように、所定の周期△Ｔごとに反転する制御信号81を信号線98を通じて出力し、また、この周期に合わせて、第１の可変フィルタ３に対して、係数Ａの値（図２（ｂ）の82）を変えて出力する。つまり、周期84には係数としてA_1 を出力し、周期85には、A_1 より所定の値△ａだけ小さいA_2 を係数として出力する。

【００４６】誤り頻度カウンタ91は、入力する制御信号が切替わるごとにカウンタ値をリセットして、△Ｔの期間にＥＣＣデコーダ７から入力するエラーフラグの数を計数する。このカウンタ値を図２（ｂ）の83に示しており、第１の可変フィルタ３が係数A_1 で等化を行なったときに時間△Ｔの間にE_1 のエラーフラグが発生し、第１の可変フィルタ３が係数A_2 で等化を行なったときにE_2 のエラーフラグが発生したことを示している。

【００４７】誤り頻度カウンタ91が期間84の最後にカウントしたエラーフラグ数E_1 は、切換スイッチ92を介してメモリ93に格納され、また、期間85の最後にカウントしたエラーフラグ数E_2 は、切換スイッチ92を介してメモリ94に格納される。判定器95は、このメモリ93及びメ

モリ94に格納されたエラーフラグ数を比較し、その値が小さいE_2に対応する係数値A_2を、最適な係数値に近いものと判定して、判定結果を係数発生器96に出力する。

$$H(f)=Z^{-1}+A(Z^{0}+Z^{-2})$$
$$=Z^{-1}\{1+2A\cdot\cos(2\pi\cdot T_1/f)\}\quad(式4)$$

（ただし、f：周波数、$Z^{-1}=\exp(-j\omega T_1)$、ω：角周波数）

となる。従って、位相特性は直線となり、係数Aの変化に対して、周波数振幅特性のみが変化する。このとき、係数Aと、ECCデコーダ7が検出する誤り頻度とは、図2（C）に示すような関係となる。

【0049】従って、係数発生器96は、判定器95から、係数値A_2（$<A_1$）の方がエラーフラグ数が少ないという判定結果を受けたときは、次の期間に、係数値A_2よりもさらに所定の値△aだけ小さい係数値を出力し、逆に、係数値A_1の方がエラーフラグ数が少ないという判定結果を受けたときは、次の期間に、係数値A_1よりもさらに△aだけ大きい係数値を出力し、このような動作を繰り返すことによって、係数Aが最適値に収束する。

【0050】こうして、この等化回路の第1の可変フィルタ3の係数及び第2の可変フィルタ4の係数が共に最適値に収束することによって、正確な等化が可能になる。

【0051】ただ、この回路では、係数Aが変化すると、第1の可変フィルタ3から出力される信号の周波数スペクトラムが変化し、そのために、第2の可変フィルタ4の特性もそれに併せて変化する。従って、第1の可変フィルタ3の係数及び第2の可変フィルタの係数が共に変化している途中の段階で誤り頻度を検出してしまうと、係数Aと、ECCデコーダが検出する誤り頻度との間に、図2（C）に示す関係が成り立たなくなる虞れがある。

【0052】これを避けるためには、第1の方法として、第2の可変フィルタ4の各係数が再帰的に最適値に収束するまでの時間を△Tcとするとき、図2（b）における所定の周期△Tを、△Tcの影響が無視できる程度に、十分長い周期に設定する方法がある。

【0053】第2の方法として、誤り頻度カウンタ91において、リセットされてから時間△Tcが経過するまでの間、エラーフラグを計数しないようにする方法がある。

【0054】また、第3の方法としては、第2の可変フィルタ4の各係数が収束したことを第2の係数計算回路6において検出して、検出結果を誤り頻度カウンタ91に伝送し、誤り頻度カウンタ91が第2の可変フィルタ4の収束を確認した後にエラーフラグの計数を開始するように構成する方法がある。この場合、第2の可変フィルタ4の各係数が収束したことを第2の係数計算回路6において検出するために、各係数の時間Tbの間の変化量を検出し、全ての係数の変化量が所定の値より小さくなったとき、第2の可変フィルタ4における係数が収束したものとして検出結果を出力させる。

【0055】こうした手段を採ることにより、第1の可変フィルタ3の収束時間は第2の可変フィルタ4の収束時間よりも長くなり、第1の可変フィルタ3は、係数の変更を行なった直後では、第2の可変フィルタ4の収束時間が経過するまで、次の係数の更新演算を行なわない。その結果、この等化回路では、第1の可変フィルタ3と第2の可変フィルタ4とが交互に収束を繰り返し、最終的に双方のフィルタの係数が共に最適値に収束する。

【0056】このように第1の可変フィルタ3の収束時間を第2の可変フィルタ4の収束時間よりも長くするということは、逆に見れば、実施例の等化回路では、第1の係数計算回路9に、第2の係数計算回路6に比較して低速で動作する回路を用いることが可能になり、その分、実現が容易になる。

【0057】また、この等化回路では、第1の可変フィルタ3の遅延器10、11における遅延時間T_1（＝Tb／2）と、第2の可変フィルタ4の遅延器20、21、22、23における遅延時間T_2（＝Tb）とを違えることによって、次に示すように、第1及び第2の可変フィルタにおける必要なタップ数の総計を減らすことを可能にしている。

【0058】図3は、第1の可変フィルタ3の周波数特性を示している。図中の点線は、遅延器10、11の遅延時間T_1をTb／2に設定した場合であり、実線は、遅延器10、11の遅延時間T_1を、第2の可変フィルタ4の遅延器と同様に、T_1＝Tbに設定した場合である。点線が示すように、遅延時間T_1がTb／2のとき、周波数特性のピークは1／Tbに現れる。一方、遅延時間T_1がTbのときは、実線が示すように、周波数特性のピークが1／（2Tb）に現れる。遅延時間Tbの遅延器を有する図4の従来の等化回路及びこの実施例の第2の可変フィルタ4における周波数特性も、この実線と同じようになり、ピーク周波数1／（2Tb）を対称点として、低周波側と高周波側とで対称の形を示す。

【0059】従って、もしも、第1の可変フィルタ3の遅延器10、11の遅延時間T_1が第2の可変フィルタ4の遅延器20～23の遅延時間Tbと同じ場合には、それらのフィルタを組合せても、実線に示す傾向の周波数特性しか得ることができない。

【００６０】一方、第１の可変フィルタ３における遅延時間を第２の可変フィルタ４の遅延時間と異ならせた場合には、それらのフィルタを組合せることによって、特に周波数１／（２Ｔｂ）から１／Ｔｂに懸けての高域帯域の周波数特性を種々に変えることができる。つまり、第１の可変フィルタ３の遅延時間と第２の可変フィルタ４の遅延時間とを変えることによって、等化特性の自由度を増すことができ、従って、少ない数のタップで所望の等化特性を得ることができる。

【００６１】これに対して、図４の従来の等化回路のタップ数を単純に増やして同程度の等化特性を得ようとすると、非常に多くのタップ数が必要になる。また、この場合には、タップ数の増加に併せて係数計算回路56の規模を大きくする必要が生じ、また、遅延回路が多く直列接続するために周波数特性の劣化が発生する。

【００６２】実施例の等化回路では、自動等化回路の可変フィルタを第１の可変フィルタ３と第２の可変フィルタ４との２段に分離することによって、遅延回路の多段直列接続による周波数劣化を避けている。

【００６３】また、実施例の等化回路は、２段の自動等化回路における係数の収束時間に差を設けることにより、２段の自動等化回路がお互いに係数の収束に悪影響を与えることを避けている。

【００６４】また、この等化回路の第１の可変フィルタ３は、位相特性が直線的で、係数Ａを変えたときに周波数振幅特性のみが可変するように構成している。この係数Ａを更新する計算回路は、ＥＣＣデコーダからのエラーフラグを基に、常に再生ディジタル信号の誤り発生が最小となるように係数を更新する。この係数の計算回路は、従来の係数計算回路に比べてその構成を簡略化できる。

【００６５】また、この等化回路では、２段の自動等化回路を、ともにトランスバーサル型の可変フィルタを用いて構成し、２つのトランスバーサルフィルタのタップ間の遅延時間をそれぞれ変えることによって、同じ等化特性を得るために必要なトータルのタップ数を削減することができる。

【００６６】なお、実施例の等化回路では、第２の可変フィルタ４のタップ数を５としたが、このタップ数を変更しても、同様の効果を得ることができる。また、第１の可変フィルタ３における遅延時間をT_1 ＝Ｔｂ／２に設定しているが、この遅延時間は、任意の値にすることができる。さらに、第１の可変フィルタ３のタップ数を３とし、可変する係数の数を１つとしたが、必ずしもこれに限られるものではなく、タップ数及び可変する係数の数をさらに多くしても良い。

【００６７】なお、実施例では、ゼロ・フォーシング法を用いた等化回路について述べたが、他のアルゴリズムを用いたものでも同様である。さらに、この等化回路は、磁気記録の再生だけでなく、光記録など、他の記録原理で記録されたデータの再生に用いたり、あるいは記録ではなく、ディジタル伝送の等化回路として用いることもできる。

【００６８】

【発明の効果】以上の実施例の説明から明らかなように、本発明の等化回路は、自動等化回路を２段に分離しているため、遅延回路の多段直列接続による周波数劣化を避けることができ、正確な等化を実現することができる。

【００６９】また、２段の自動等化回路の一方を、位相直線で、周波数振幅特性のみを可変する可変フィルタとし、また、この可変フィルタの係数をＥＣＣデコーダからのエラーフラグを用いて更新するようにしているため、このフィルタの係数計算回路の構成が簡略化できる。また、この係数計算回路は、一方の自動等化回路の収束時間を長くする必要上、動作速度が低速でも足りるため、回路の実現が容易である。

【００７０】また、２段の自動等化回路をともにトランスバーサル型の可変フィルタを用いて構成し、２つのトランスバーサルフィルタのタップ間の遅延時間を違えることによって、同じ等化特性を得るために必要なトータルのタップ数を減らすことができ、回路規模を小さく保つことができる。

【図面の簡単な説明】

【図１】本発明の実施例における等化回路の構成を示すブロック図、

【図２】実施例の等化回路の第１の係数計算回路を示すブロック図（ａ）、この第１の係数計算回路の各部の信号波形を示す図（ｂ）、第１の係数計算回路が出力する係数ＡとＥＣＣデコーダの検出する誤り頻度との関係を示す図（ｃ）、

【図３】遅延器の遅延時間を変えたときの第１の可変フィルタの周波数特性における変化を示す図、

【図４】従来の等化回路の構成を示すブロック図、

【図５】再生ヘッドから出力される信号の信号スペクトラム図、

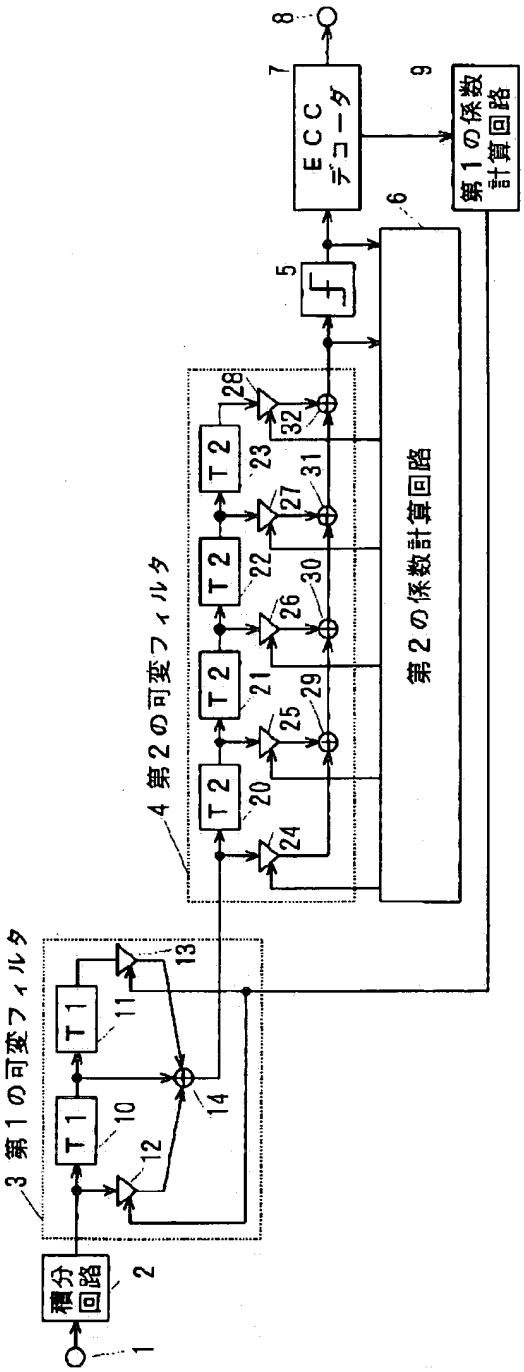
【図６】従来の等化回路における係数計算回路を示すブロック図である。

【符号の説明】

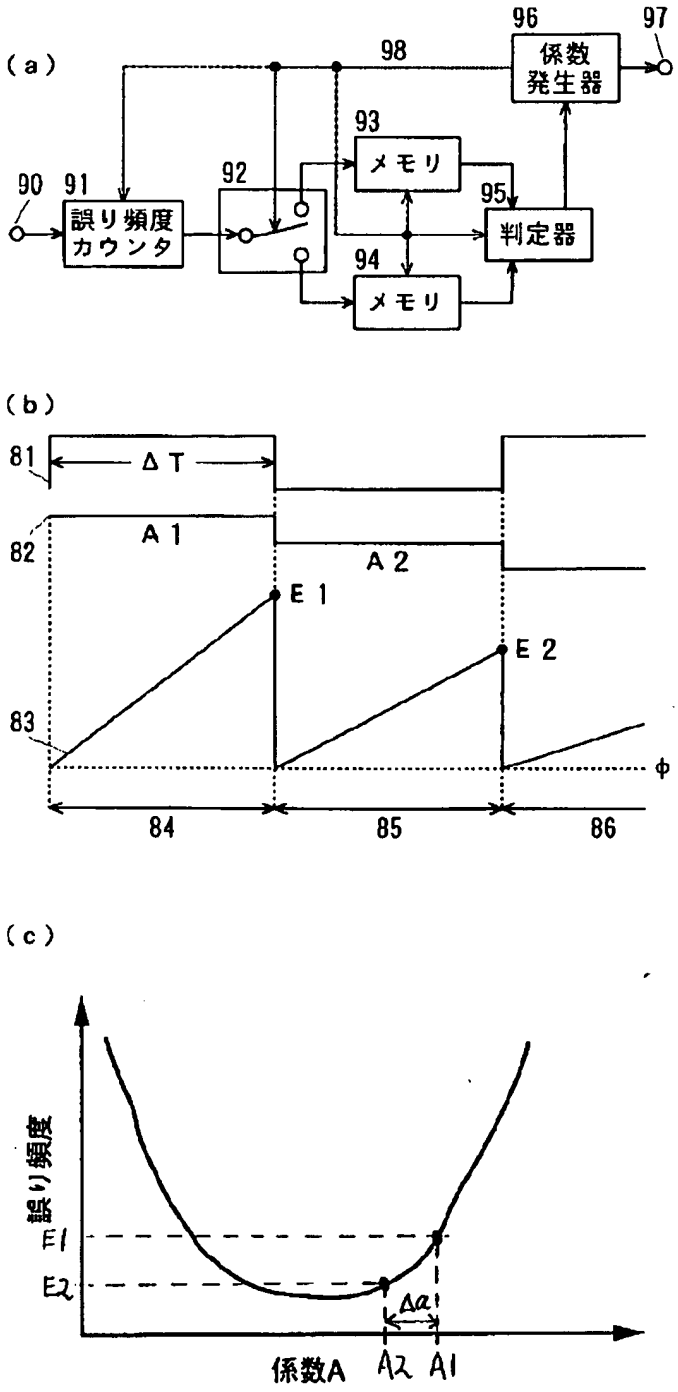
１　入力端子
２、45　積分回路
３　第１の可変フィルタ
４　第２の可変フィルタ
５、55　識別回路
６　第２の係数計算回路
７　ＥＣＣデコーダ
８、54、57、97　出力端子
９　第１の係数計算回路
10、11、20～23　遅延器
12、13、24～28　可変利得増幅回路

14、29～32、53　加算器
41　磁気テープ
42　再生ヘッド
43　等化回路
44、47、61、62、90　入力端子
46　トランスバーサルフィルタ
48、49、64、68、69　遅延回路
50～52　可変利得増幅器
56　係数計算回路
63　減算器
65～67　計算回路
82　係数A
83　誤り頻度カウンタ91からの出力信号
91　誤り頻度カウンタ
92　切換スイッチ
93、94　メモリ
95　判定器
96　係数発生器

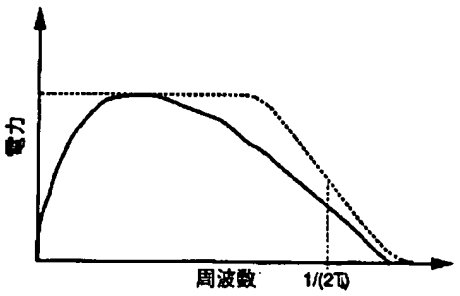
【図1】



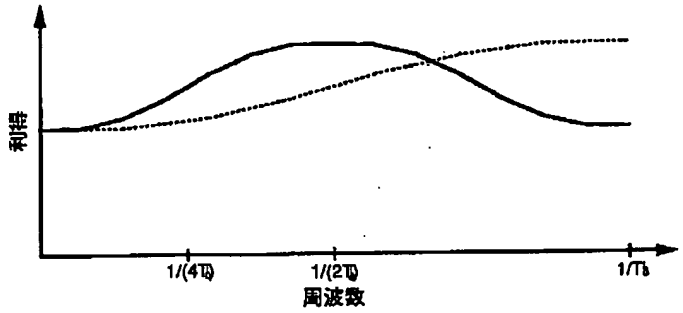
【図2】


(a)
90
91
誤り頻度
カウンタ
92
93
メモリ
94
メモリ
95
判定器
96
係数
発生器
97
98
(b)
81
ΔT
82
A1
A2
E1
E2
83
φ
84
85
86
(c)
誤り頻度
E1
E2
Δα
係数A
A2
A1

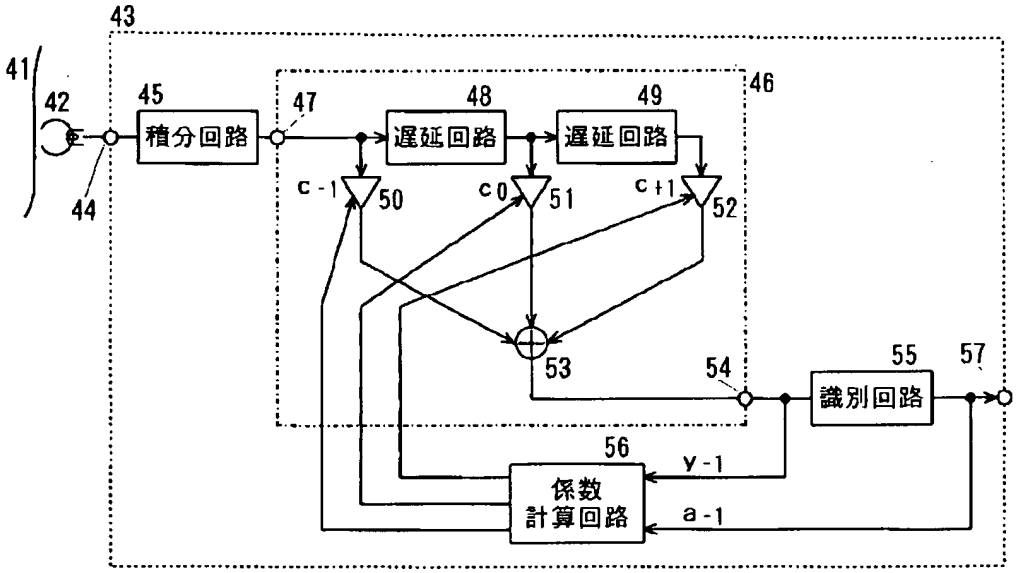
【図5】


電力
周波数
1/(2T)

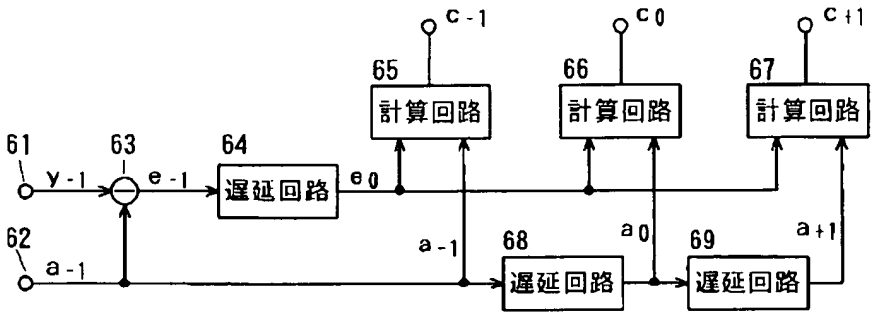
【図3】


利得
1/(4Tb)
1/(2Tb)
1/Tb
周波数

【図4】


43
41
42
44
45
積分回路
47
48
遅延回路
49
遅延回路
46
c-1
50
c0
51
c+1
52
53
54
55
識別回路
57
56
係数
計算回路
y-1
a-1

【図6】


c-1
c0
c+1
65
計算回路
66
計算回路
67
計算回路
61
y-1
63
e-1
64
遅延回路
e0
62
a-1
a-1
68
遅延回路
a0
69
遅延回路
a+1